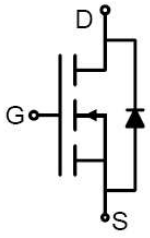
TP85N04Q

N-CHANNEL ENHANCEMENT MOSFET

Feature

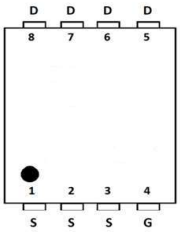
40V,65A
$R_{DS(ON)}$ <5.9mΩ @V_{GS}=10V TYP 5.0 mΩ
$R_{DS(ON)}$ <10mΩ @V_{GS}=4.5V TYP 7.5 mΩ
Advanced Trench Technology
Lead free product is acquired
Excellent $R_{DS(ON)}$ and Low Gate Charge



Schematic Diagram

Application

PWM applications
Load Switch
Power management



Marking and pin Assignment

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity (PCS)
85N04Q	TP85N04Q	PDFN3X3-8L	13 inch	-	5000

ABSOLUTE MAXIMUM RATINGS (T_a=25℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current (T_a =25℃)	I_D	65	A
Continuous Drain Current (T_a =100℃)	I_D	41	A
Pulsed Drain Currenr (1)	I_{DM}	260	A
Singel Pulsed Avalanche Energy (2)	E_{AS}	96	mJ
Power Dissipation	P_D	48	W
Thermal Resistance from Junction to Case(4)	$R_{\theta JC}$	2.6	℃/W
Junction Temperature	T_J	150	℃
Storage Temperature	T_{STG}	-55~ +150	℃

MOSFET ELECTRICAL CHARACTERISTICS(T_a=25℃ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Type	Max	Unit
Static Characteristics						
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D =250μA	40	-	-	V
Zero gate voltage drain current	I_{DSS}	V_{DS} =40V, V_{GS} = 0V	-	-	1	μA
Gate-body leakage current	I_{GSS}	V_{GS} =±20V,V_{DS} = 0V	-	-	±100	nA
Gate threshold voltage(3)	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D =250μA	1	1.5	2.5	V
Drain-source on-resistance(3)	$R_{DS(on)}$	V_{GS} =10V, I_D =30A	-	5.0	5.9	mΩ
		V_{GS} =4.5V, I_D =20A	-	7.5	10	
Dynamic characteristics						
Input Capacitance	C_{iss}	V_{DS} =20V, V_{GS} =0V, f =1MHz	-	2956	-	pF
Output Capacitance	C_{oss}		-	225	-	
Reverse Transfer Capacitance	C_{rss}		-	197	-	
Switching characteristics						
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V, I_D=30A, R_L=1Ω V_{GS}=10V, R_G=3Ω	-	8	-	ns
Turn-on rise time	t_r		-	16	-	
Turn-off delay time	$t_{d(off)}$		-	21	-	
Turn-off fall time	t_f		-	10	-	
Total Gate Charge	Qg	VDS=20V, ID=30A, VGS=10V	-	46	-	nC
Gate-Source Charge	Qgs		-	7.2	-	
Gate-Drain Charge	Qgd		-	8.8	-	
Source-Drain Diode characteristics						
Diode Forward voltage(3)	V_{DS}	V_{GS} =0V, I_S=1A	-	-	1.2	V
Diode Forward current(4)	I_S		-	-	65	A

Notes:

1. Repetitive Rating: pulse width limited by maximum junction temperature
2. EAS Condition:T_J=25℃,V_{DD}=20V,R_G=25Ω,L=0.5mH
3. Pulse Test: pulse width≤300μs, duty cycle≤2%
4. Surface Mounted on FR4 Board,t≤10 sec

Test Circuit

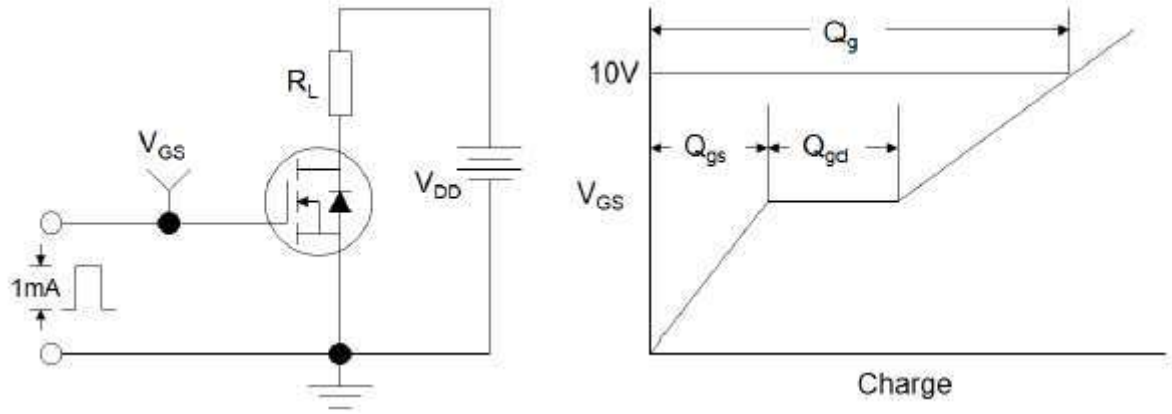


Figure1:Gate Charge Test Circuit & Waveform

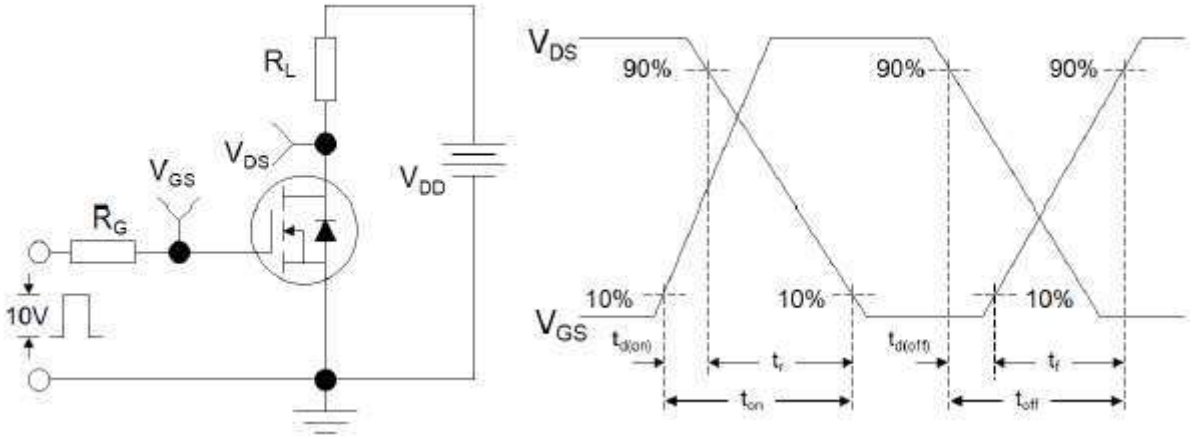


Figure 2: Resistive Switching Test Circuit & Waveforms

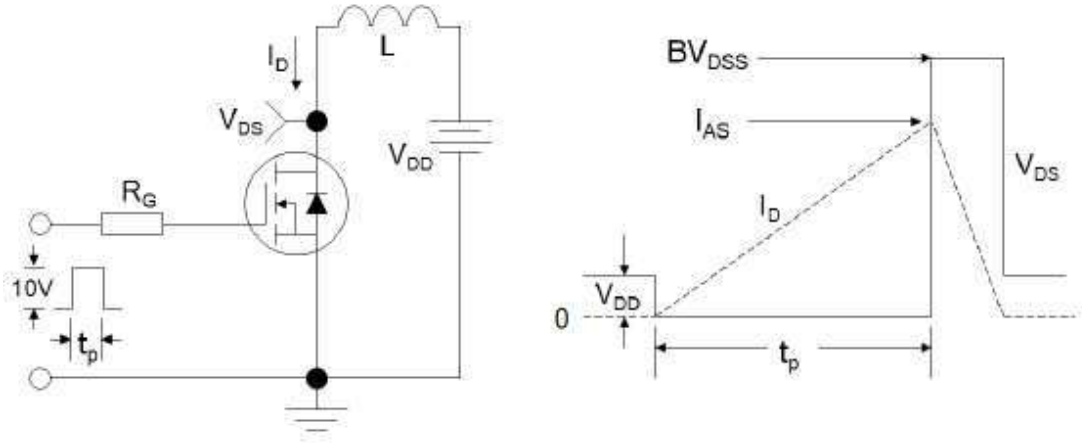


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Figure1: Output Characteristics

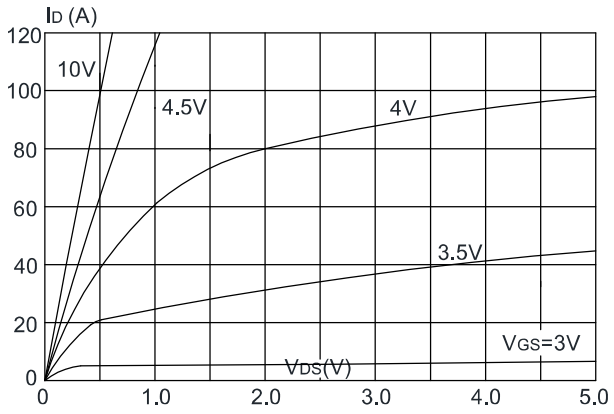


Figure 2: Typical Transfer Characteristics

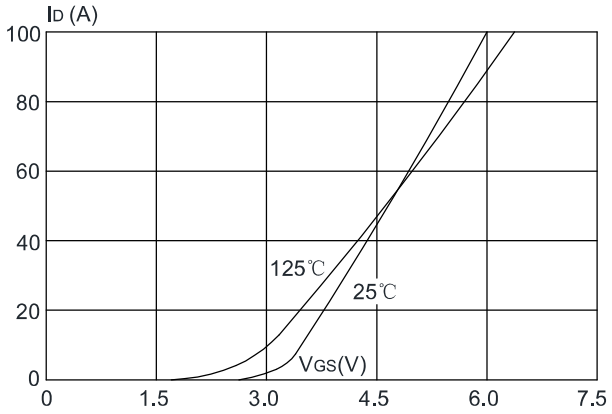


Figure 3: On-resistance vs. Drain Current

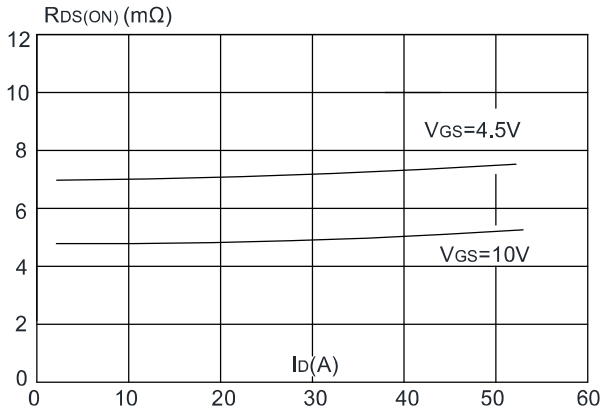


Figure 4: Body Diode Characteristics

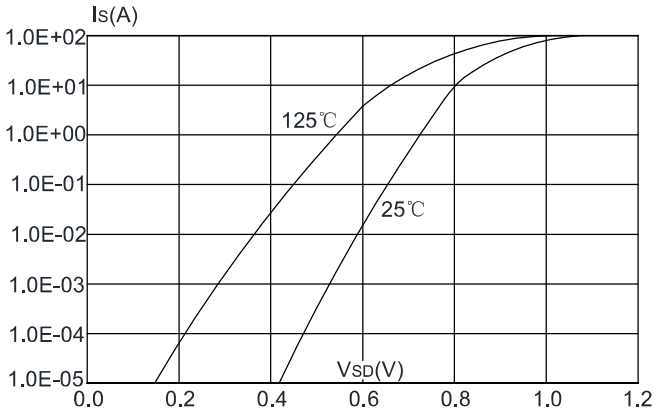


Figure 5: Gate Charge Characteristics

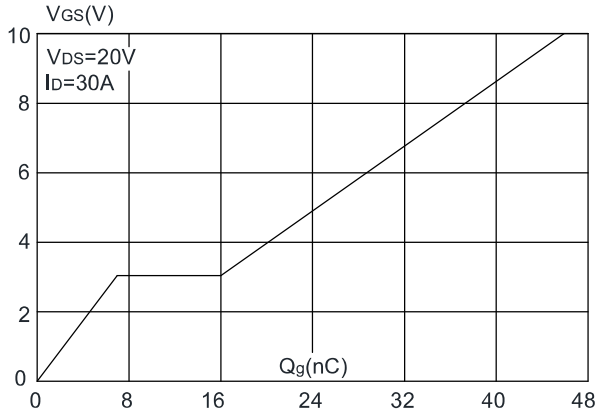


Figure 6: Capacitance Characteristics

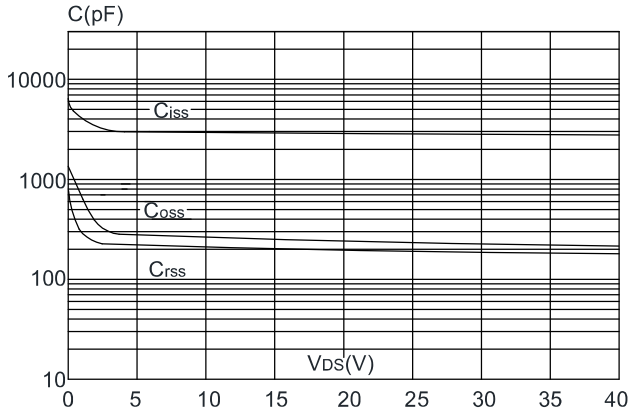


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

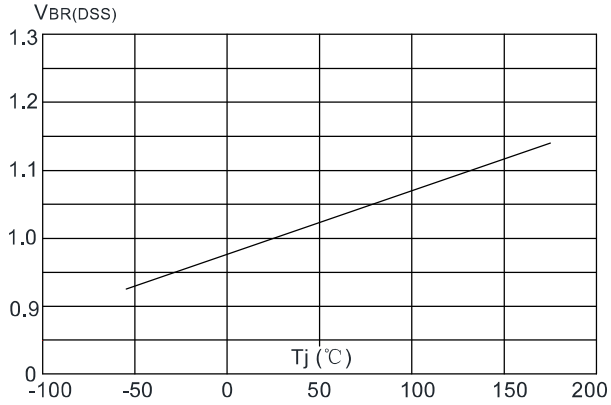


Figure 8: Normalized on Resistance vs. Junction Temperature

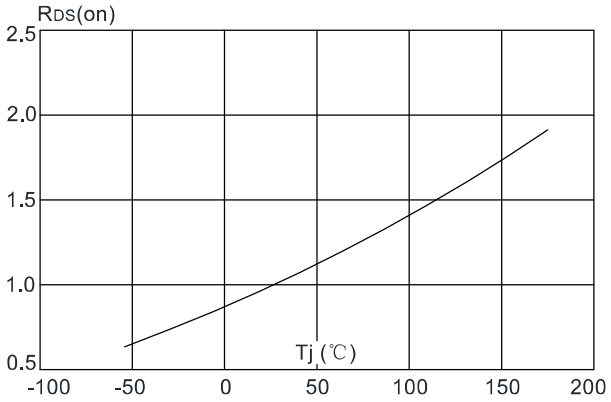


Figure 9: Maximum Safe Operating Area

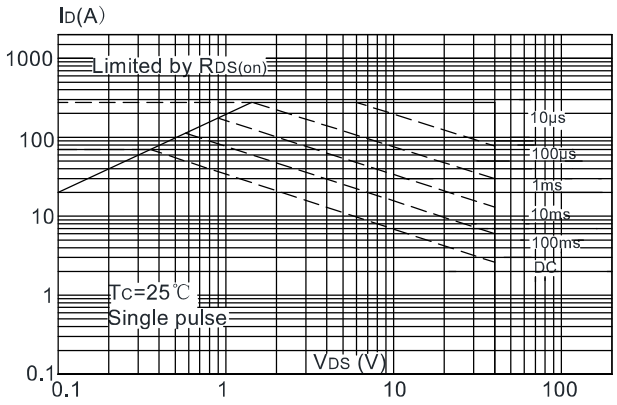


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

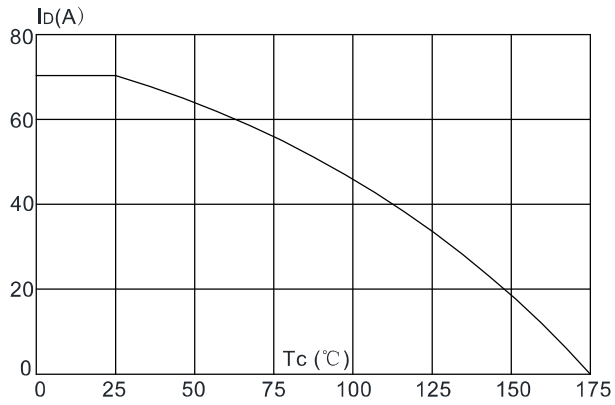
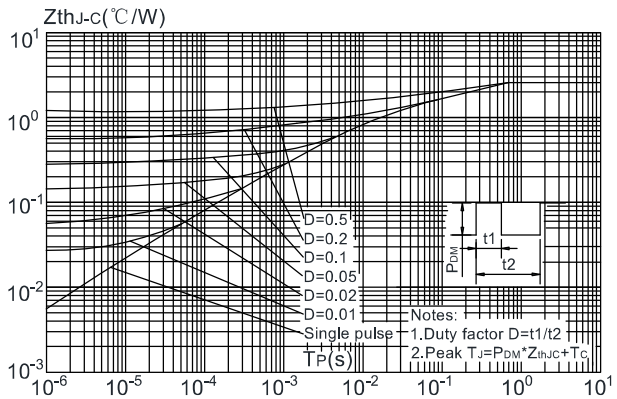
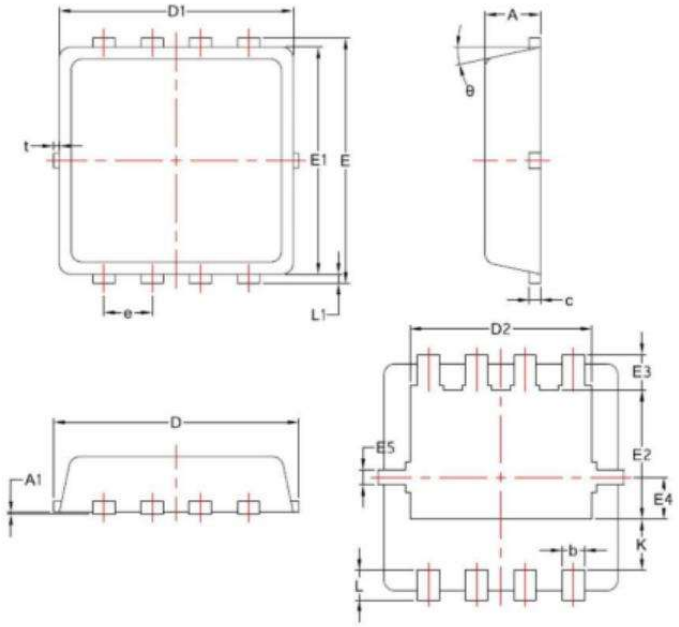


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



PDFN3X3-8L Package Information



SYMBOL	COMMON		
	MM		
	MIN	NOM	MAX
A	0.70	0.75	0.85
A1	/	/	0.05
b	0.20	0.30	0.40
c	0.10	0.152	0.25
D	3.15	3.30	3.45
D1	3.00	3.15	3.25
D2	2.29	2.45	2.65
E	3.15	3.30	3.45
E1	2.90	3.05	3.20
E2	1.54	1.74	1.94
E3	0.28	0.48	0.65
E4	0.37	0.57	0.77
E5	0.10	0.20	0.30
e	0.60	0.65	0.70
K	0.59	0.69	0.89
L	0.30	0.40	0.50
L1	0.06	0.125	0.20
t	0	0.075	0.13
θ	10°	12°	14°