TPA20957 Protected Digital Audio Driver

1 Features

- Floating PWM Input
- Programmable bidirectional over-current protection with self-reset function
- External 5V reference voltage output, low voltage side overcurrent protection threshold programmable
- Programmable preset deadtime for improved THD performances
- High noise immunity：> 50 V/ns
- ±100 V ratings deliver up to 500 W in output power
- Operates up to 800KHz
- Wide temperature range：-40 ℃ ~125 ℃
- Dynamical electrical characteristics：
  - High and low side propagation delay：90/105ns
  - OC protection delay (max)：500ns
  - Shutdown propagation delay (max)：250ns
- Output high short circuit current (Source/Sink) up to 2A
- RoHS compliant

2 RoHS compliant

- Home theatre systems
- Mini component stereo systems
- Powered speaker systems
- General purpose audio power amplifiers

3 Description

The TPA20957 is a high voltage, high speed MOSFET driver with a floating PWM input designed for Class D audio amplifier applications.

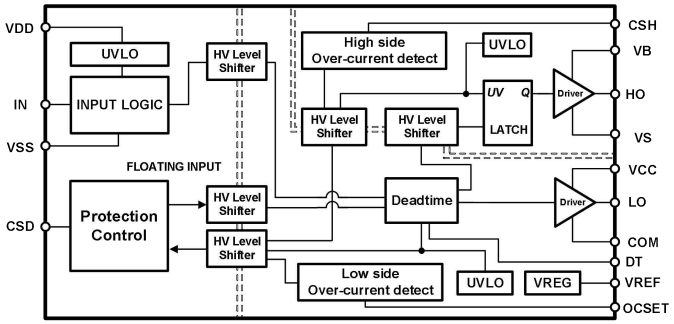
Bi-directional current sensing detects over current conditions during positive and negative load currents without any external shunt resistors. A built-in protection control block provides a secure protection sequence against over-current conditions and a programmable reset timer.

The internal dead-time generation block enables accurate gate switching and optimum dead-time setting for better audio performance, such as lower THD and lower audio noise floor.

Device information

Part Number	Package	Body size
TPA20957	SOIC16 (S)	9.9 mm X 3.9 mm

Functional Block Diagram



4 Ordering Guide

Part Number	LOGO	Package	Package	SPQ
TPA20957	A20957 XXXXXX	SOIC16(S)	Tape & Reel	4000

5 Revision history

Version	Content	Time
V1.0	Create	2021.11.29
V2.0	Product features and application information	2022.03.05

6 Function Pin Description

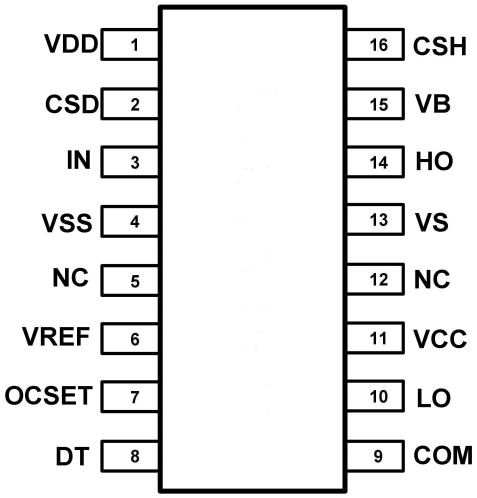


Figure6-1 16-Pin SOIC Top view

Table6-1 Lead Definitions

PIN NO.	Name	Type	Function
1	VDD	POWER	Floating input positive supply
2	CSD	GROUND	Floating input supply return
3	IN-	INPUT	Analog inverting input
4	VSS	POWER	Floating input negative supply
5	NC		
6	VREF	OUTPUT	5V reference voltage to program OCSET pin
7	OCSET	INPUT	Low side over current threshold setting
8	DT	INPUT	Deadtime program input
9	COM	GROUND	Low side supply return
10	LO	OUTPUT	Low side output
11	VCC	POWER	Low side supply
12	NC		
13	VS	GROUND	High side floating supply return
14	HO	OUTPUT	High side output
15	VB	POWER	High side floating supply
16	CSH	INPUT	High side over current sensing input

7 Product specifications

7.1 Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM; all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply voltage	-0.3	315	V
V_S	High side floating supply voltage [I]	V_B -15	V_B + 0.3	
V_{HO}	High side floating output voltage	V_S -0.3	V_B + 0.3	
V_{CSH}	CSH pin input voltage	V_S -0.3	V_B + 0.3	
V_{CC}	Low side fixed supply voltage [I]	-0.3	20	
V_{LO}	Low side output voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Floating input positive supply voltage	-0.3	310	
V_{SS}	Floating input negative supply voltage [I]	See I_{DDZ}	V_{DD}+0.3	
V_{IN}	PWM pin input voltage	V_{SS}-0.3	V_{DD}+0.3	
V_{CSD}	CSD pin input voltage	V_{SS}-0.3	V_{DD}+0.3	
V_{DT}	DT pin input voltage	-0.3	V_{CC}+0.3	
V_{OCSET}	OCSET pin input voltage	-0.3	V_{CC}+0.3	
V_{REF}	VREF pin voltage	-0.3	V_{CC}+0.3	
I_{DDZ}	Floating input positive supply zener clamp current [I]	—	10	mA
I_{CCZ}	Floating input negative supply zener clamp current [I]	—	10	
I_{BSZ}	Low side supply zener clamp current [I]	—	10	
I_{OREF}	Floating supply zener clamp current [I]	—	5	
dV_S/dt	Reference output current	—	50	V/ns
dVss/dt	Allowable Vs voltage slew rate [II]	—	50	
dVss/dt	Allowable V_{SS} voltage slew rate upon power-up [III]	—	50	V/ms

I V_{DD}-V_{SS}, V_{CC}-COM and V_B-V_S contain internal shunt zener diodes. Please note that the voltage ratings of these can be limited by the clamping current.

II For the rising and falling edges of step signal of 10V. V_{SS}=15V to 300V

III V_{SS} ramps up from 0V to300V

7.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	750	—	V
	Machine Model	200	—	V

7.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	1	W

7.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	115	°C /W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

7.5 Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions below. The Vs and COM offset ratings are tested with supplies biased at I_{DD}=5mA, V_{CC}=12V and V_B-V_S=12V.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply absolute voltage	V_S +10	V_S +14	V
V_S	High side floating supply offset voltage	— I	300	
I_{DDZ}	Floating input positive supply zener clamp current	1	5	mA
V_{SS}	Floating input supply absolute voltage	0	300	V
V_{HO}	High side floating output voltage	V_S	V_B	
V_{CC}	Low side fixed supply voltage	10	18	
V_{LO}	Low side output voltage	0	V_{CC}	
V_{IN}	PWM pin input voltage	V_{SS}	V_{DD}	
V_{CSD}	CSD pin input voltage	V_{SS}	V_{DD}	
V_{DT}	DT pin input voltage	0	V_{CC}	
I_{OREF}	Reference output current to COM I	0.3	0.8	mA
V_{OCSET}	OCSET pin input voltage	0.5	5	V
T_A	Ambient Temperature	-40	125	°C

I Logic operational for Vs equal to –5V to +300V. Logic state held for Vs equal to –5V to –VBS.

II Nominal voltage for VREF is 5V. IOREF of 0.3 – 0.8mA dictates total external resistor value on VREF to be 6.3k to 16.7k Ω.

7.6 Electrical Characteristics

Valid for temperature range at TA= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified.

7.6.1 Low side suply

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
UV_{CC+}	Vcc supply UVLO positive threshold	8.40	8.90	9.40	V	
UV_{CC-}	Vcc supply UVLO negative threshold	8.20	8.70	9.20		
I_{QCC}	Low side quiescent current	—	—	3	mA	V_{DT}=V_{CC}
V_{clampL}	Low side zener diode clamp voltage	19.6	20.4	21.6	V	I_{CC}=5mA

7.6.2 High Side Floating Supply

Symbol	Definition		MIN.	TYP.	MAX.	Units	Test Condition
UV_{BS+}	High side well UVLO positive threshold		8	8.5	9.0	V	
UV_{BS-}	High side well UVLO negative threshold		7.8	8.3	8.8		
I_{QBS}	High side quiescent current		—	—	1	mA	
I_{LKH}	High to Low side leakage current		—	—	50	uA	V_B=V_S=300V
V_{ClampH}	High side zener diode clamp voltage	TPA2095X	14.7	15.3	16.2	V	I_{BS}=5mA
		TPA20955	19.6	20.4	21.6		

7.6.3 Floating Input Supply

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
UV_{DD+}	V_{DD}, V_{SS} floating supply UVLO positive threshold	8.2	8.7	9.2	V	V_{SS}=0V
UV_{DD-}	V_{DD}, V_{SS} floating supply UVLO negative threshold	7.7	8.2	8.7		V_{SS}=0V
I_{QDD}	Floating Input quiescent current	—	—	1	mA	V_{DD}=9.5V+V_{SS}
V_{CLAMPM}	Floating Input zener diode clamp voltage	9.8	10.2	10.8	V	I_{DD}=5mA
I_{LKM}	Floating input side to Low side leakage current	—	—	50	uA	V_{DD}=V_{SS} =300V

7.6.4 Floating PWM Input

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{IH}	Logic high input threshold voltage	2.3	1.9	—	V	
V_{IL}	Logic low input threshold voltage	—	1.9	1.5		
I_{IN+}	Logic “1” input bias current	—	—	40	uA	V_{IN}=3.3V
I_{IN-}	Logic “0” input bias current	—	—	1		V_{IN}=V_{SS}

7.6.5 Protection

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{ref}	Reference output voltage	4.8	5.1	5.4	V	I_{oREF}=0.5mA
V_{thOCL}	Low side OC threshold in Vs	1.1	1.2	1.3		OCSET=1.2V
V_{thOCH}	High side OC threshold in V_{CSH}	1.1+V_S	1.2+V_S	1.3+V_S		V_S=300V
V_{th1}	CSD pin shutdown release threshold	0.62V_{DD}	0.7V_{DD}	0.78V_{DD}		V_{SS}=0V
V_{th2}	CSD pin self reset threshold	0.26V_{DD}	0.30V_{DD}	0.34V_{DD}		V_{SS}=0V
I_{CSD+}	CSD pin discharge current	70	100	130	uA	V_{SD}=V_{SS}+5V
I_{CSD-}	CSD pin charge current	70	100	130		V_{SD}=V_{SS}+5V
t_{sd}	Propagation delay time from V_{CSD}<V_{th2} to Shutdown	—	—	250	ns	
t_{och}	Propagation delay time from V_{csh}>V_{vthoch} to Shutdown	—	—	500		
t_{ocl}	Propagation delay time from V_s>V_{thocl} to Shutdown	—	—	500		

7.6.6 Gate Driver

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
I_{O+}	Output high short circuit current (Source)	—	2	—	A	V_O=0V, PW<10us
I_{O-}	Output low short circuit current (Sink)	—	2	—		V_O=12V, PW<10us
V_{OL}	Low level out put voltage LO – COM, HO - VS	—	—	0.1	V	Io=0
V_{OH}	High level out put voltage VCC – LO, VB - HO	—	—	1.4		Io=0
t_r	Turn-on rise time	—	15	—	ns	
t_f	Turn-off fall time	—	10	—		
T_{on_1}	High and low side turn-on propagation delay, floating inputs	—	105	—		V_{DT}=V_{CC} V_S=100V V_{SS}=100V
T_{off_1}	High and low side turn-off propagation delay, floating inputs	—	95	—		V_{DT}=V_{CC} V_S=100V V_{SS}=100V
T_{on_2}	High and low side turn-on non-propagation delay, floating inputs	—	105	—		
T_{off_2}	High and low side turn-off non-propagation delay, floating inputs	—	95	—		
DT1	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	8	15	22		V_{DT}>V_{DT1} V_{SS}=COM
DT2	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	15	25	35		V_{DT1}>V_{DT}>V_{DT2} V_{SS}=COM
DT3	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	20	35	50		V_{DT2}>V_{DT}>V_{DT3} V_{SS}=COM
DT4	Deadtime: LO turn-off to HO turn-on (DT_{LO-HO}) & HO turn-off to LO turn-on (DT_{HO-LO})	50	80	110		V_{DT3}>V_{DT} V_{SS}=COM
V_{DT1}	DT mode select threshold 1	0.51Vcc	0.57Vcc	0.63Vcc	V	
V_{DT2}	DT mode select threshold 2	0.32Vcc	0.36Vcc	0.40Vcc		
V_{DT3}	DT mode select threshold 3	0.21Vcc	0.23Vcc	0.25Vcc		

8 Waveform definitions

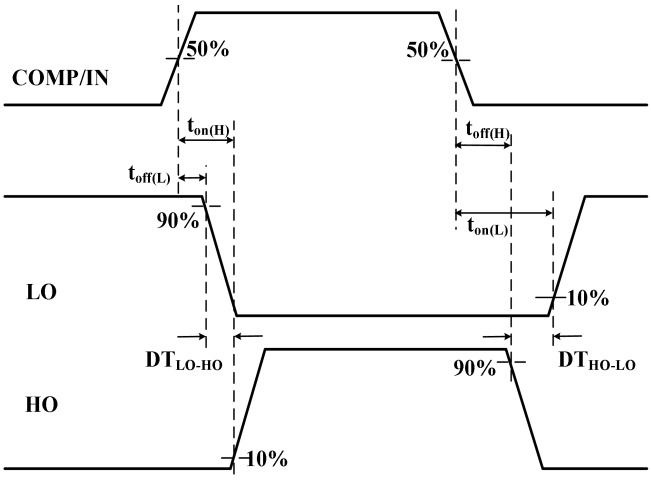


Figure 8-1. Switching Time Waveform Definitions

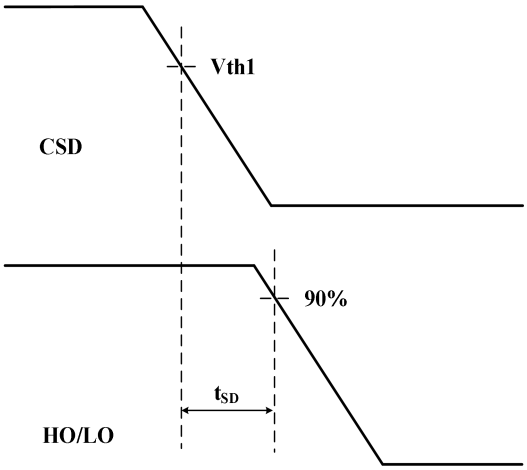


Figure 8-2. CSD to Shutdown Waveform Definitions

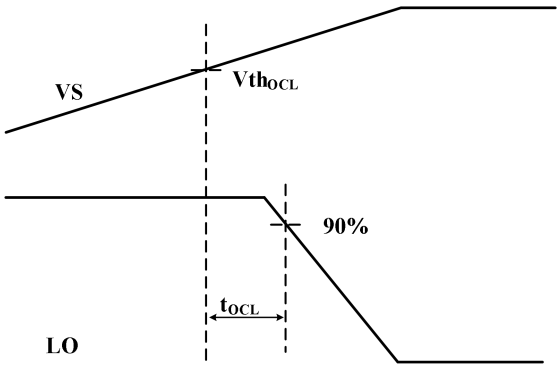


Figure 8-3. VS > VthOCL to Shutdown Waveform

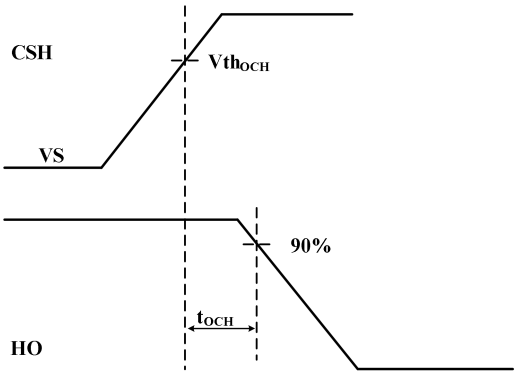


Figure 8-4. VCSH > VthOCH to Shutdown Waveform

9 Input/Output Pin Equivalent Circuit Diagrams

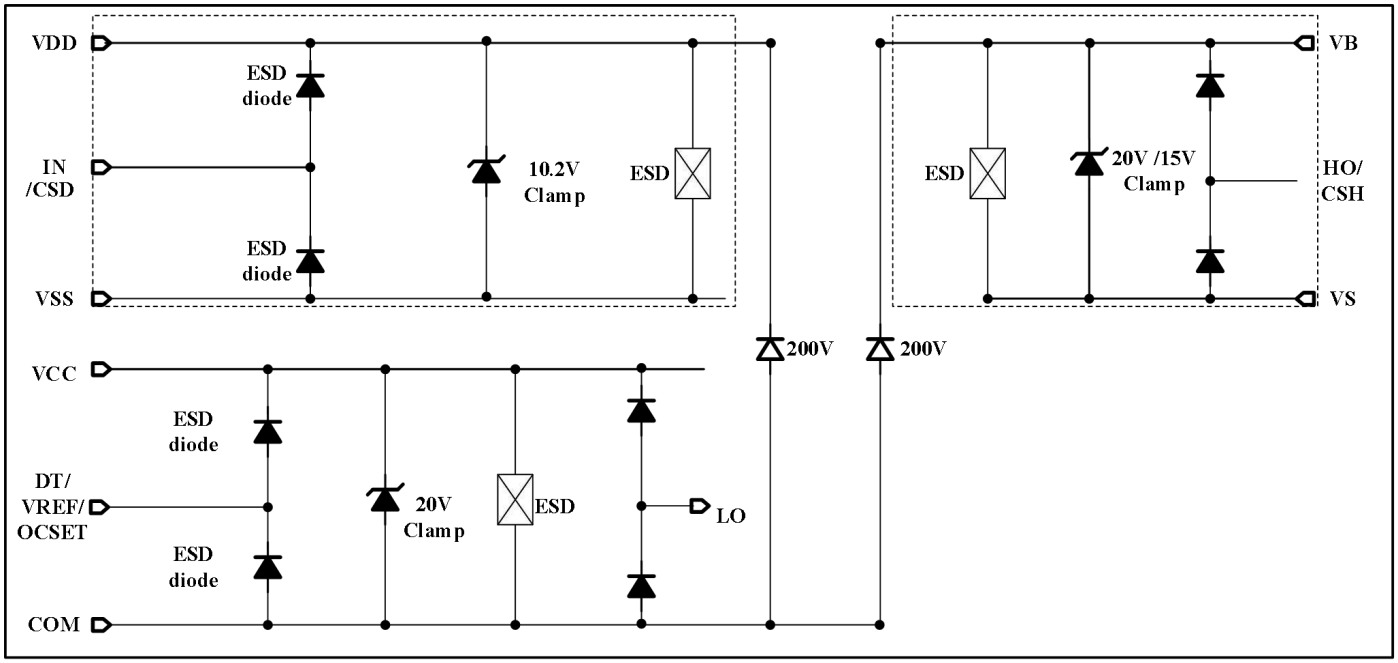


Figure 9-1 Input/Output Pin Equivalent Circuit

10 General Description

10.1 Functional Description

TPA20957 is a high power Class D audio amplifier driver chip with integrated overcurrent protection. The TPA20957 chip combines an error amplifier, two external power MOSFETs and some passive devices to form a complete Class D audio power amplifier with high and low voltage side overcurrent protection, through protection and undervoltage protection. TPA20957 chip in the absence of any external shunt resistor, the bidirectional current detection function can detect the overcurrent during the positive and negative load current, for overcurrent conditions built-in protection control module to provide safety protection timing and programmable reset timer; This product detects whether the power device is overcurrent by detecting the $R_{DS(on)}$ of the power MOSFET, which abandons the traditional way of directly detecting the current under overcurrent protection, simplifies the system structure, and reduces the complexity of the application.

Figure 10-1 shows the TPA20957 full-chip functional block diagram. To match the bridge output structure, the analog PWM input and protection logic are placed in a floating trap, and the high-voltage side circuit is also placed in a floating trap. The breakdown voltage between the floating trap and the chip substrate (COM) exceeds 300V, which can be used for power amplifier applications up to ±150V. Achieve more than 500W of power output.

10.2 Functional Block Diagram

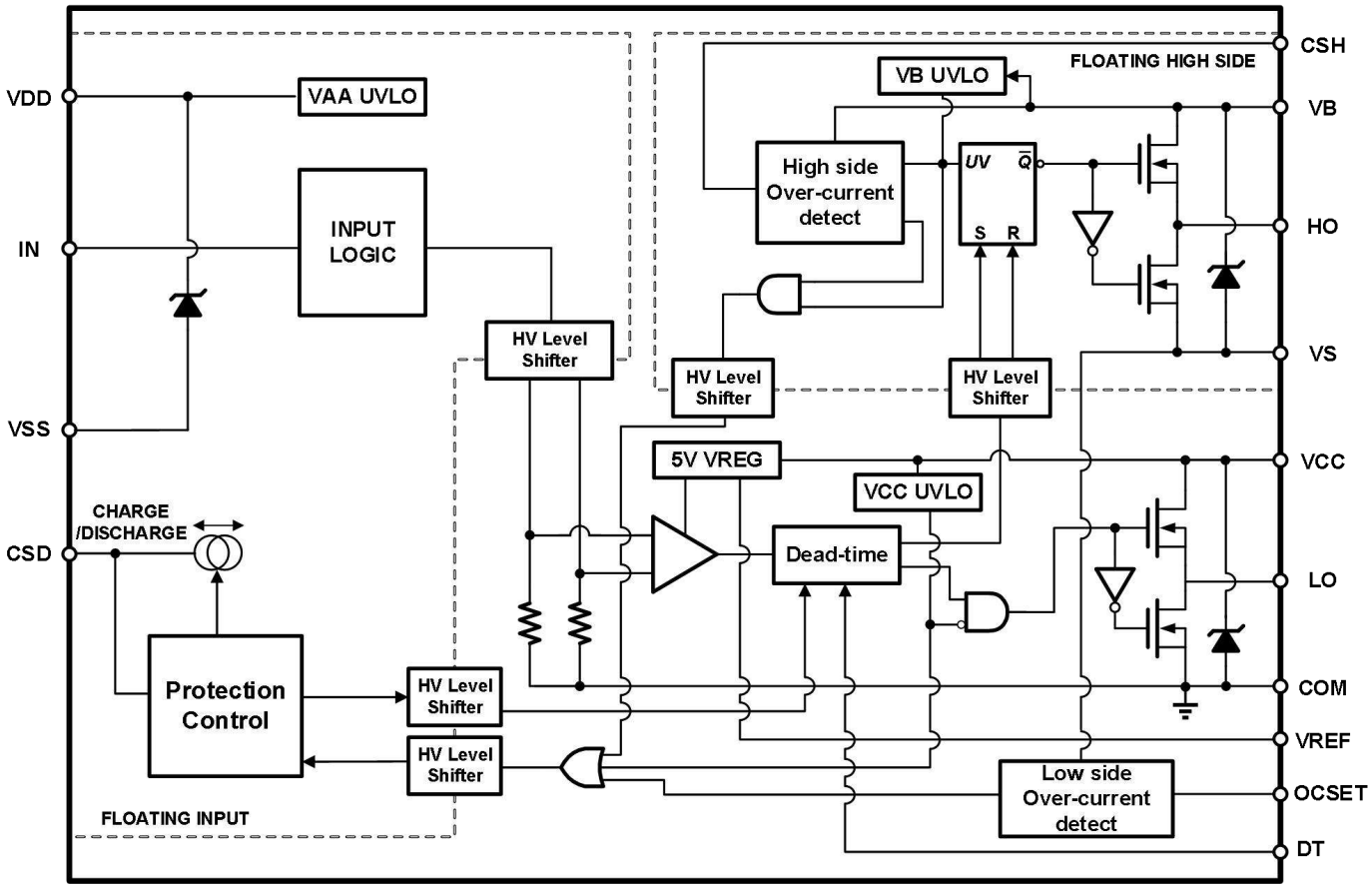


Figure10-1 Functional Block Diagram

10. 3 Typical Connection Diagram

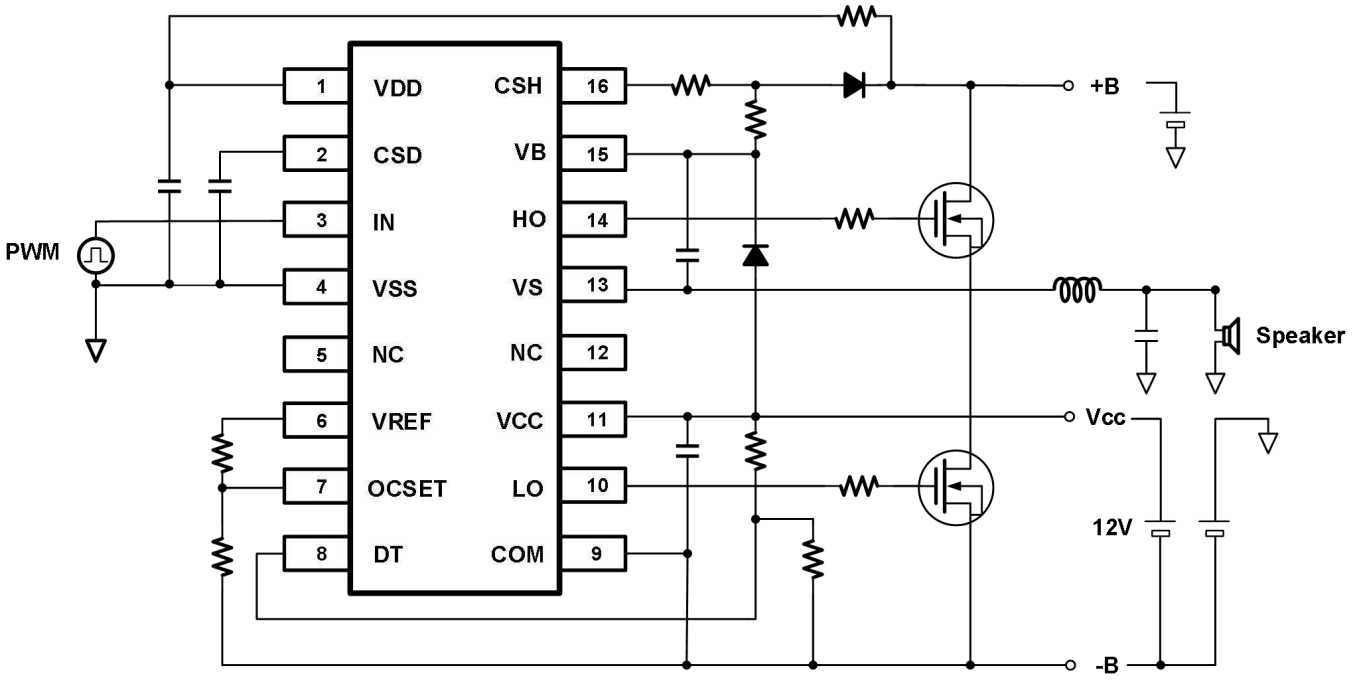


Figure10-2 Typical Connection Diagram

10. 4 Floating PWM Input

The TPA20957 accepts floating inputs, enabling easy half-bridge implementation. V_{DD}, CSD and IN refer to V_{SS}. As a result, the PWM input signal can directly feed into IN while referencing V_{SS}, which is typically the midpoint between the positive and negative DC bus voltages in a half-bridge configuration. The TPA20957 also accepts a non-floating input when V_{SS} is tied to COM.

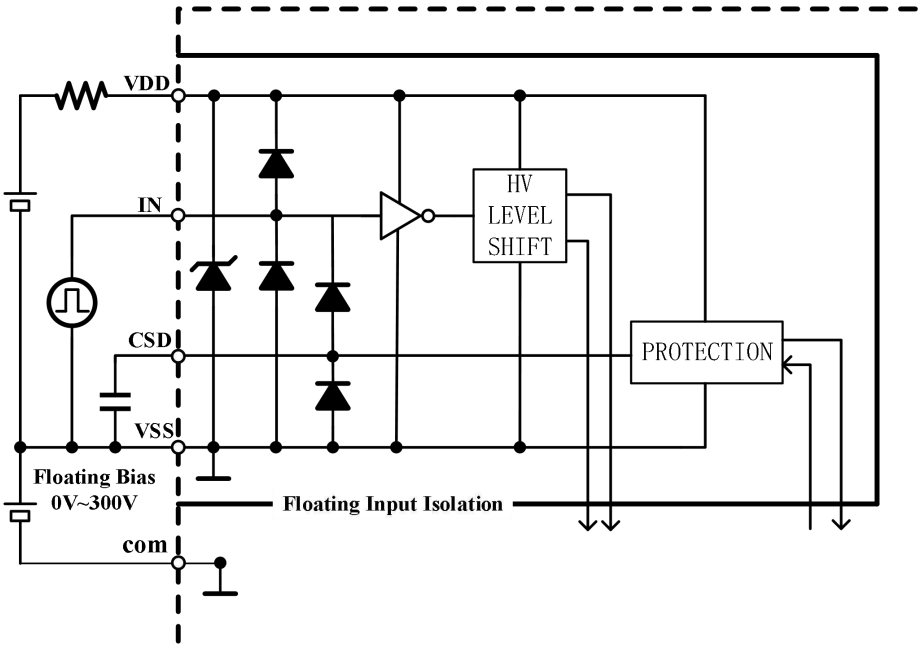


Figure10-3 Floating PWM Input Structure

10.5 Low-side Over-Current Sensing

For negative load currents, low-side over-current sensing monitors the load condition and shuts down switching operation if the load current exceeds the preset trip level.

Low-side current sensing is based on the measurement of VDS across the low side MOSFET during low-side turn on. In order to avoid triggering OCP from overshoot, a blanking interval inserted after LO turn on disables over-current detection for 450 ns.

The OCSET pin is used to program the threshold for low-side over-current sensing. When the VDS measured across the low-side MOSFET exceeds the voltage at the OCSET pin with respect to COM, the TNSA20957 begins the OCP sequence described earlier.

Note that programmable OCSET range is 0.5V to 5.0V. To disable low side OCP, connect OCSET to VCC directly.

To program the trip level for over current, the voltage at OCSET can be calculated using the equation below.

$V_{OCSET}=V_{DS(LOW\ SIDE)}=I_{TRIP}+XR_{DS(ON)}$

In order to minimize the effect of the input bias current at the OCSET pin, select resistor values for R4 and R5 such that the current through the voltage divider is 0.5 mA or more.

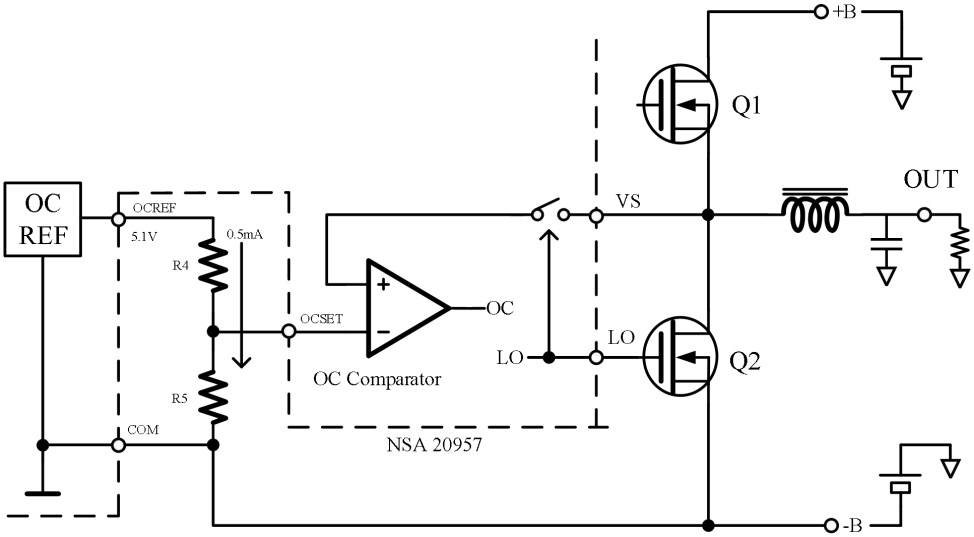


Figure10-4 Low-Side Over-Current Sensing

10.6 Over-Current Protection

The TPA20957 features over-current protection to protect the power MOSFETs during abnormal load conditions.

The TPA20957 starts a sequence of events when it detects an over-current condition during either high-side or low-side turn on of a pulse.

As soon as either the high-side or low-side current sensing block detects over-current:

（1）The OC Latch (OCL) flips logic states and shutdowns the outputs LO and HO.

（2）The CSD pin starts discharging the external capacitor Ct.

（3）When VCSD, the voltage across Ct, falls below the lower threshold Vth2, an output signal from COMP2 resets OCL.

（4）When VCSD goes above the upper threshold Vth1, the logic on COMP1 flips and the IC resumes operation.

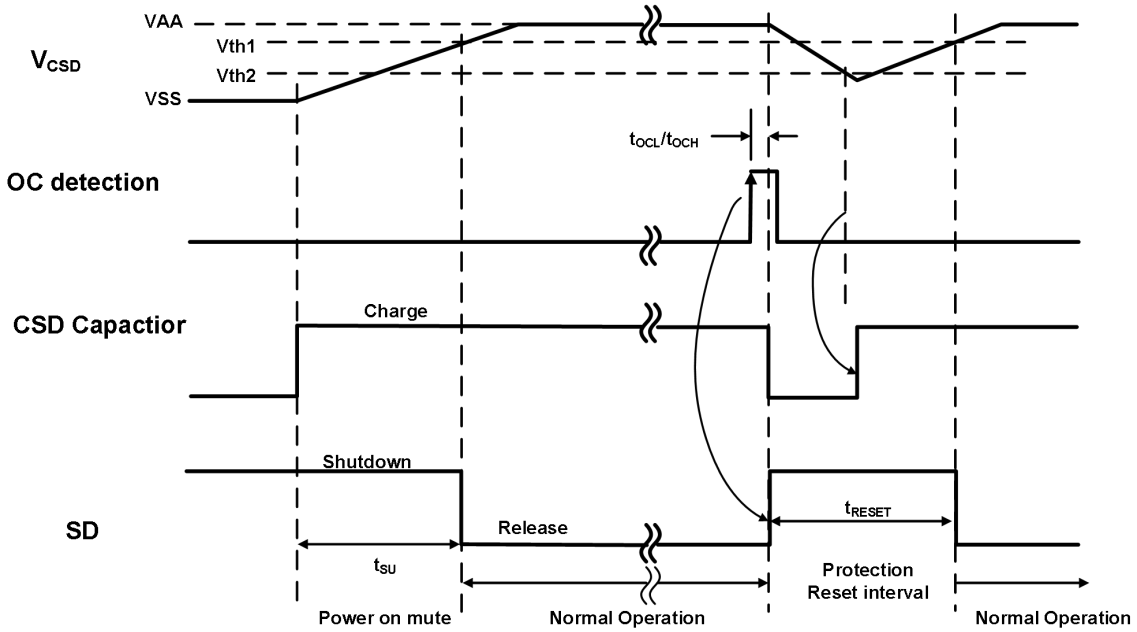


Figure10-5 Over-Current Protection Timing Chart

10.7 Programming Dead-Time

The TPA20957 selects the deadtime from a range of preset deadtime values based on the voltage applied at the DT pin. An internal comparator translates the DT input to a predetermined deadtime by comparing the input with internal reference voltages. These internal reference voltages are set in the IC through a resistive voltage divider using VCC. The relationship between the operation mode and the voltage at DT pin is illustrated in the Figure10-6 below.

When V_{DT} < 0.23VCC, DT = 80ns;

When 0.23VCC < V_{DT} < 0.36VCC, DT = 35ns;

When 0.36VCC < V_{DT} < 0.57VCC, DT = 25ns;

When 0.57VCC < V_{DT} < VCC, DT = 15ns.

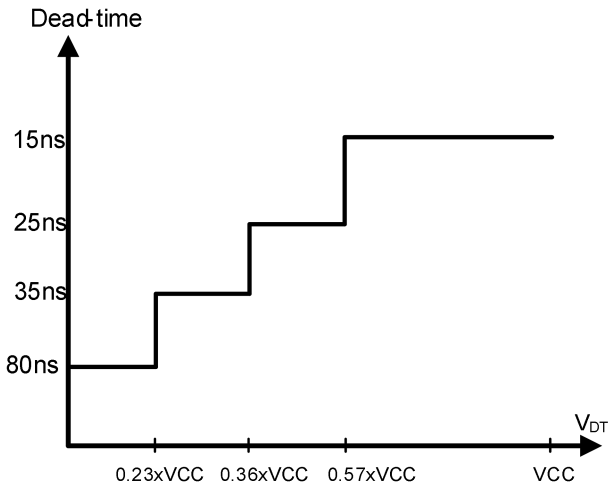


Figure10-6 Dead Time vs. V_{DT}

11 Package Information

SOIC16 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	9.70	9.90	10.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	L	0.25	-	0.50
b1	0.38	0.41	0.43	L1		1.4BSC	
c	0.21	-	0.26	θ	0	-	8°
c1	0.19	0.20	0.21				

SOIC16 Package Outlines