TPG2103 700V High side & Low side MOSFET/IGBT Gate Driver

1 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700V
- 3.3 V, 5V and 15V logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability = -9V
- VCC Undervoltage Lockout circuit
  -- Undervoltage reset threshold=8.9V
  -- Undervoltage set threshold= 8.2V
- Transmission characteristic
  -- turn-on/turn-off Propagation delay
  Ton/Toff =650ns/130ns
  -- Delay matching=50ns
- Cross-conduction prevention logic
  -- Deadtime:520ns
- Wide operating temperature range -40°C ~125°C
- Output Source/ Sink current 300mA/600mA
- RoSH compatible
  SOIC8 (S)

2 Application

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

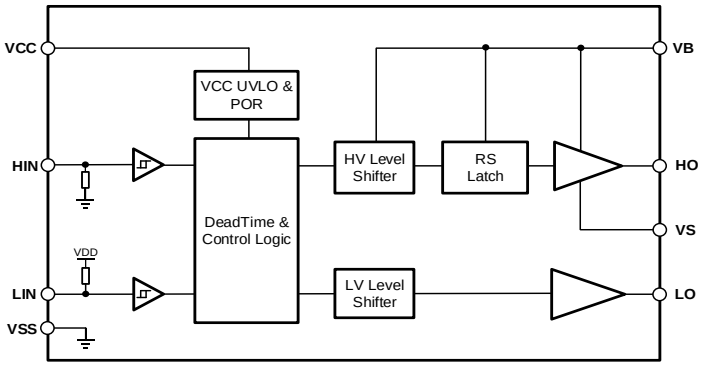
3 Description

The TPG2103 is a high voltage, high speed power MOSFET drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

Device information

Part Number	Package	Body size
TPG2103	SOIC8	4.9mm x 3.9mm

Functional Block Diagram



4 Selection Guide

Part Number	Input signal	Shout-though prevention	Deadtime	VBS UVLO	Ton/Toff (ns)	IO+/IO- (mA)
TPG2103	HIN, $\overline{\text{LIN}}$	YES	520ns	NO	650/130	300/600

5 Ordering Guide

Part Number	LOGO	Package	Package	SPQ
TPG2103	G2103 XXXXX	SOIC8	Tape & Reel	4000

6 Revision history

Version	Content	Time
V1.0	Create	2021.04.01

7 Function Pin Description

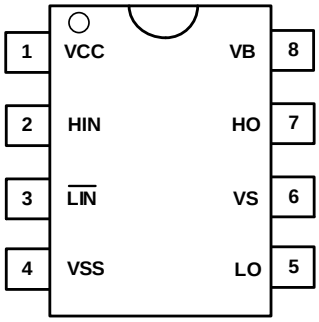


Figure7-1 8-Pin SOIC8 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	VCC	Low side and logic fixed supply
2	HIN	Logic input for high side gate driver output (HO), in phase
3	$\overline{\text{LIN}}$	Logic input for low side gate driver output (LO), out of phase
4	VSS	Low side return
5	LO	Low side gate drive output
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

8 Product specifications

8.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to VSS and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	725	V
V_S	High side floating supply return	V_B – 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of HIN & $\overline{LIN}$	-0.3	V_{CC} + 0.3	
dV_S/dt	Allowable Offset Supply Voltage Transient	—	50	V/ns

8.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1500	—	V
	Machine Model	500	—	V

8.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
PD1	Package Power Dissipation @ TA ≤25°C	—	625	mW

8.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	--	200	°C/W
T_J	Junction Temperature	—	150	
T_S	Storage Temperature	-55	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	°C/W

8.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	V_S + 10	V_S + 20	V
V_S	High side floating supply return	-9	700	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of HIN & $\overline{LIN}$	0	V_{CC}	
T_A	Ambient temperature	-40	125	°C

Note1：Transient negative VS can be used for VSS-50V with a pulse width of 50ns, guaranteed by design..

8.6 Electrical Characteristics

8.6.1 Dynamical electrical characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	650	820	ns	V_S=0V
t_{OFF}	Turn-off propagation delay	—	130	200	ns	V_S=700V
t_R	Turn-on rise time	—	75	130	ns	
t_F	Turn-off fall time	—	35	70	ns	
DT	Deadtime	400	520	650	ns	
MT	Matching delay ON and OFF	—	—	50	ns	
MDT	Matching delay	—	—	60	ns	

8.6.2 Static electrical characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0	V	
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—	V	
I_{LK}	Leakage current from VS (600V) to GND	—	—	50	μA	V_B=V_S=700V
I_{QBS}	Quiescent VB supply current	—	50	100	μA	V_{IN}=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	120	240	μA	V_{IN}=0V or 5V
V_{IH}	Logic “1”(HIN&$\overline{LIN}$) input voltage	2.5	—	—	V	VCC=10V to 20V
V_{IL}	Logic “0” (HIN&$\overline{LIN}$) input voltage	—	—	0.8	V	VCC=10V to 20V
V_{OH}	High level output voltage, VBIAS - VO	—	—	0.1	V	I_O=0A
V_{OL}	Low level output voltage, VO	—	—	0.1	V	I_O=0A
I_{IN+}	Logic “1” Input bias current	—	5	10	μA	HIN=5V, $\overline{LIN}$=0V
I_{IN-}	Logic “0” Input bias current	—	—	2	μA	HIN=0V, $\overline{LIN}$=5V
I_{O+}	Output high short circuit pulsed current	200	300	—	mA	V_O=0V PW≤10us
I_{O-}	Output low short circuit pulsed current	400	600	—	mA	V_O=15V PW≤10us

9 Function Description

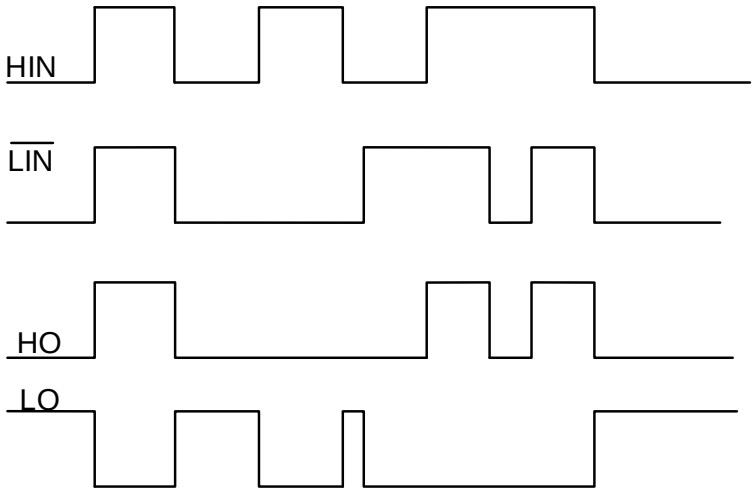


Figure 5. TPG2103 Input and output timing waveform

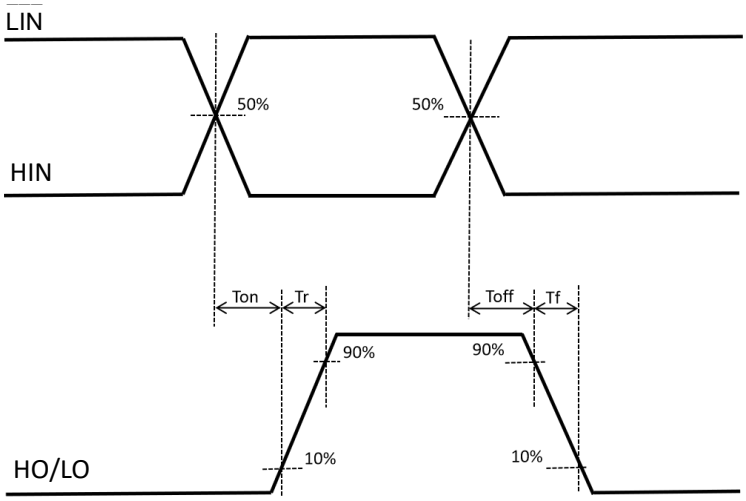


Figure 6. Propagation Time Waveform Definition

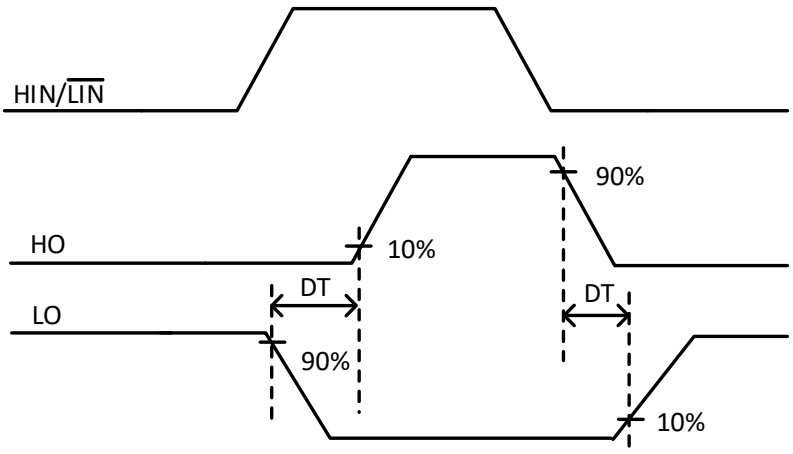


Figure7. Cross Conduction Prevention Delay Time Waveform Definition

10 TPG2103 Description

10.1 Function Block Diagram

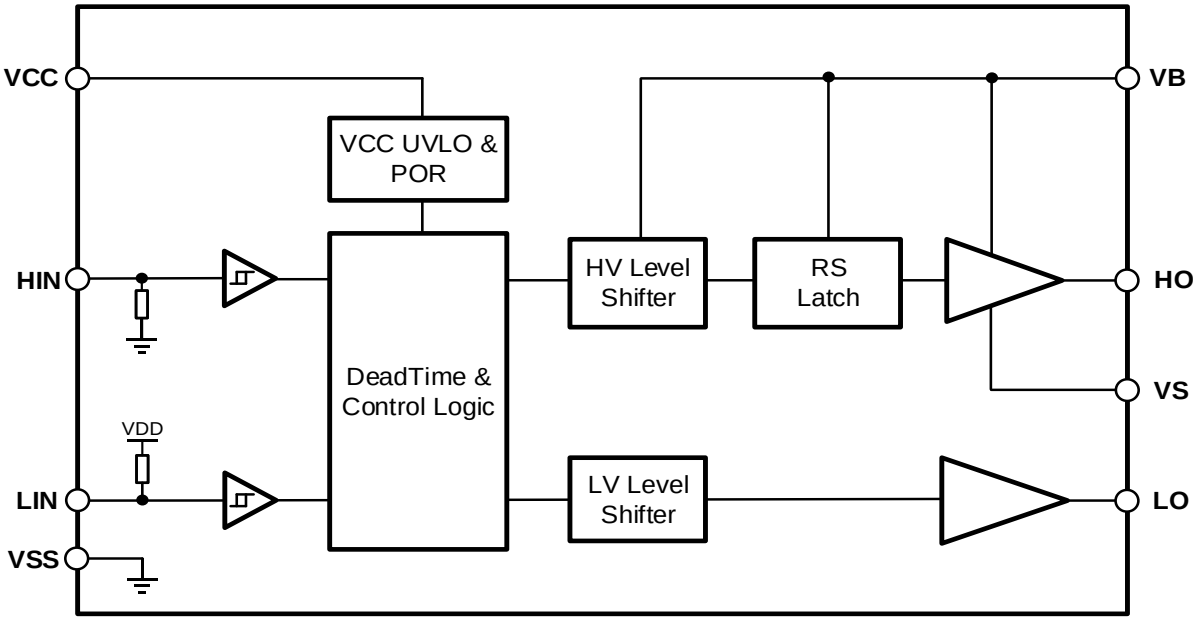


Figure10-1 Function Block Diagram of TPG2103

10.2 Typical application circuit

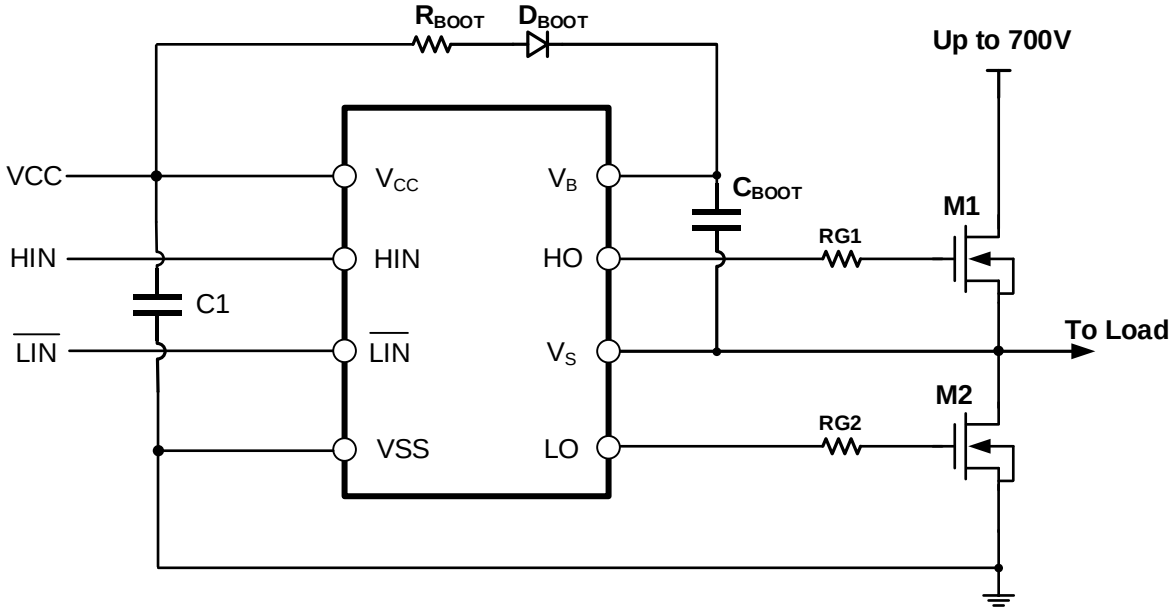


Figure10-2 Typical application circuit of TPG2103

11.Package Information

SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e	1.27BSC		
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L	0.50	-	0.80
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

SOIC-8 Package Outlines