TPG2136 700V three-phase gate driver IC with OCP, Enable, and Fault

1 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- Tolerant to negative transient voltage dV/dt immune
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Integrated advanced input filtering
- The input of all transmission channels is edge-triggered
- Undervoltage lockout for all channels
- Cross-conduction prevention logic
- Over-current shutdown turns off all six drivers
- Independent 3 half-bridge drivers
- Matched propagation delay for all channels
- Integrated bootstrap diode
- RoHS Compliant

2 Typical Applications

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

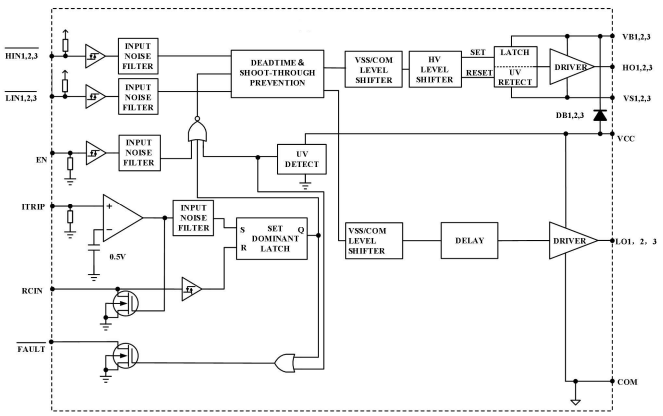
3 Description

TPG2136 is a high voltage, high speed power MOSFET and IGBT drivers with three independent high and low side referenced output channels for 3-phase applications. A current trip function which terminates all six outputs can be derived from an external current sense resistor. An enable function is available to terminate all six outputs simultaneously. Over current fault conditions are cleared automatically after a delay programmed externally via an RC network connected to the RCIN input. TPG2136 s integrated with a bootstrap diode to charge the high side, simplifying the peripheral circuit of the chip. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

Device information

Part Number	Package	Body size
TPG2136	SOP28	18mm x 7.5mm

Functional Block Diagram



4 Selection Guide

Version 1.1, 2022.10.10

Part No.	High-side input	Low-side input	Anti-cross	Dead-time	VBS UVLO	Ton/Toff (ns)	IO+/IO- (A)
TPG2136	$\overline{HIN}_{1,2,3}$	$\overline{LIN}_{1,2,3}$	YES	290ns	YES	500/500	0.45/0.7

5 Ordering Guide

Part Number	Package	Package	SPQ
TPG2136	SOP28	Tape & Reel	1000

6 Revision history

Version	Content	Time
V1.0	Create	2022.07.15
V1.1	Added function description	2022.10.10

7 Function Pin Description

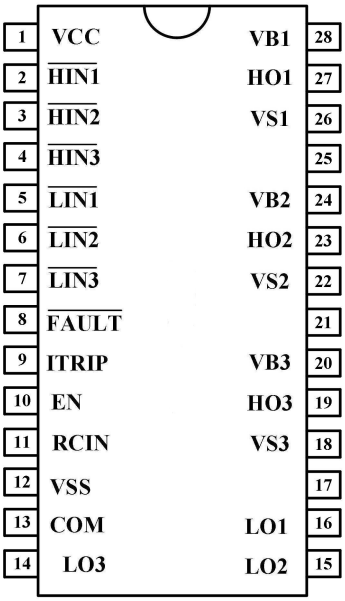


Figure7-1 28-Pin SOP Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	VCC	Low side and logic fixed supply
2	$\overline{\text{HIN1}}$	Logic inputs for high side gate driver output , out of phase
3	$\overline{\text{HIN2}}$	Logic inputs for high side gate driver output , out of phase
4	$\overline{\text{HIN3}}$	Logic inputs for high side gate driver output , out of phase
5	$\overline{\text{LIN1}}$	Logic inputs for low side gate driver output , out of phase
6	$\overline{\text{LIN2}}$	Logic inputs for low side gate driver output , out of phase
7	$\overline{\text{LIN3}}$	Logic inputs for low side gate driver output , out of phase
8	$\overline{\text{FAULT}}$	Indicates over-current (ITRIP) or low-side under voltage lockout has occurred. Negative logic, open drain output, out of phase
9	ITRIP	Analog input for over current shutdown.
10	EN	Logic input to enable I/O functionality.
11	RCIN	External RC network input used to define FAULT clear delay
12	VSS	Logic ground
13	COM	Low side gate drivers return
14	LO3	Low side gate driver output
15	LO2	Low side gate driver output
16	LO1	Low side gate driver output
18	VS3	High voltage floating supply return
19	HO3	High side gate driver output
20	VB3	High side floating supply
22	VS2	High voltage floating supply return
23	HO2	High side gate driver output
24	VB2	High side floating supply
26	VS1	High voltage floating supply return
27	HO1	High side gate driver output
28	VB1	High side floating supply

8 Product specifications

8.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
$V_{B1,2,3}$	High side floating supply	-0.3	725	V
$V_{S1,2,3}$	High side floating supply return	$V_{B1,2,3}$ - 25	$V_{B1,2,3}$ + 0.3	
$V_{HO1,2,3}$	High side gate drive output	$V_{S1,2,3}$ -0.3	$V_{S1,2,3}$ + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
$V_{LO1,2,3}$	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input of $\overline{HIN}_{1,2,3}$ & $\overline{LIN}_{1,2,3}$&EN	V_{SS}-0.3	V_{CC} + 0.3	
V_{SS}	Logic ground	V_{CC}-25	V_{CC}+0.3	
V_{RCIN}	RCIN input voltage	V_{SS}-0.3	V_{CC}+0.3	
V_{FAULT}	$\overline{FAULT}$ output voltage	V_{SS}-0.3	V_{CC}+0.3	
dV_S/dt	Allowable offset voltage slew rate	—	50	V/ns

8.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	2000	—	V
	Machine Model	500	—	V

8.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	625	mW

8.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	200	°C/W
T_J	Junction Temperature	—	150	
T_S	Storage Temperature	-55	150	°C
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	°C/W

8.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
$V_{B1,2,3}$	High side floating supply	VS +10	VS +20	V
$V_{S1,2,3}$	High side floating supply return	-9	700	
$V_{HO1,2,3}$	High side gate drive output	$V_{S1,2,3}$	$V_{B,1,2,3}$	
V_{CC}	Low side and main power supply	10	20	
$V_{LO1,2,3}$	Low side gate drive output	0	V_{CC}	
V_{IN}	Logic input of $\overline{HIN}_{1,2,3}$ & $\overline{LIN}_{1,2,3}$&EN	0	V_{CC}	
VSS	Logic ground	-5	5	
V_{RCIN}	RCIN input voltage	V_{SS}	V_{CC}	
V_{FAULT}	$\overline{FAULT}$ output voltage	V_{SS}	V_{CC}	
T_A	Allowable offset voltage slew rate	-40	125	°C

8.6 Electrical Characteristics

Valid for temperature range at T_A= 25°C, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

8.6.1 Dynamical electrical characteristics

Symbol	Definition		MIN.	TYP.	MAX.	Units
t_{ON}	Turn-on propagation delay		350	500	750	ns
t_{OFF}	Turn-off propagation delay		350	500	750	
t_R	Turn-on rise time		—	60	130	
t_F	Turn-off fall time		—	40	90	
t_{EN}	ENABLE low to output shutdown propagation delay		250	400	520	
t_{ITRIP}	ITRIP to output shutdown propagation delay		350	470	590	
t_{bl}	ITRIP blanking time		—	400	—	
t_{FLT}	ITRIP to $\overline{FAULT}$ propagation delay		400	625	950	
t_{FLTIN}	Input filter time	negative pulse	250	350	—	
		positive pulse	250	350	—	
$t_{filterEN}$	The input filtering time of enabled		170	250	—	
DT	Deadtime		190	290	420	
MT	Matched propagation time delay		—	—	50	
MDT	Matched deadtime delay		—	—	60	
PM	Output pulse width matching (pwin-pwout)		—	—	75	
t_{FLTCLR}	FAULT clear time RCIN: R = 2 MΩ, C = 1nF		1.3	1.6	2	ms

8.6.2 Static electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units
V_{IH}	Logic “1”($HIN_{1,2,3}$&$LIN_{1,2,3}$) input voltage	2.5	—	—	V
V_{IL}	Logic “0” ($HIN_{1,2,3}$&$LIN_{1,2,3}$) input voltage	—	—	0.8	
$V_{EN,TH+}$	Enable positive going threshold	—	—	2.5	
$V_{EN,TH}$	Enable negative going threshold	0.8	—	—	
$V_{IT,TH+}$	ITRIP positive going threshold	0.37	0.46	0.55	
$V_{IT,HYS}$	ITRIP input hysteresis	—	0.06	—	
$V_{RCIN,TH+}$	RCIN positive going threshold	—	8	—	
$V_{RCIN,HYS}$	RCIN input hysteresis	—	3	—	
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	—	0.3	
V_{OL}	Low level output voltage, V_O	—	—	0.3	
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	8.2	8.9	9.6	
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	—	8.2	—	
$V_{CCUVHYS}$	V_{CC} supply undervoltage lockout hysteresis	—	0.7	—	
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	8.2	8.9	9.6	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	—	8.2	—	
$V_{BSUVHYS}$	V_{BS} supply undervoltage lockout hysteresis	—	0.7	—	
$V_{IN,CLAMP}$	Input clamp voltage (HIN, LIN, ITRIP and EN)	5.5	6	6.55	
I_{LK}	Offset supply leakage current	—	—	50	μA
I_{QBS}	Quiescent VB supply current	—	60	150	
I_{QCC}	Quiescent VCC supply current	—	160	250	
I_{IN+}	Logic “1” Input bias current	—	12	50	
I_{IN-}	Logic “0” Input bias current	—	120	240	
I_{ITRIP+}	“High” ITRIP input bias current	—	6	15	
I_{ITRIP-}	“Low” ITRIP input bias current	—	—	1	
I_{EN+}	“High” ENABLE input bias current	—	6	15	
I_{EN-}	“Low” ENABLE input bias current	—	—	1	
I_{RCIN}	RCIN input bias current	—	—	1	
I_{O+}	Output high short circuit pulsed current	120	210	—	mA
I_{O-}	Output low short circuit pulsed current	250	350	—	
R_{on_RCIN}	RCIN low on resistance	—	30	80	Ω
R_{on_FAULT}	$\overline{FAULT}$ low on resistance	—	30	80	
V_{BSD}	Bootstrap diode conduction voltage	—	0.6	—	V
R_{BSD}	Bootstrap diode conduction resistance	—	200	—	Ω

9 Function Description

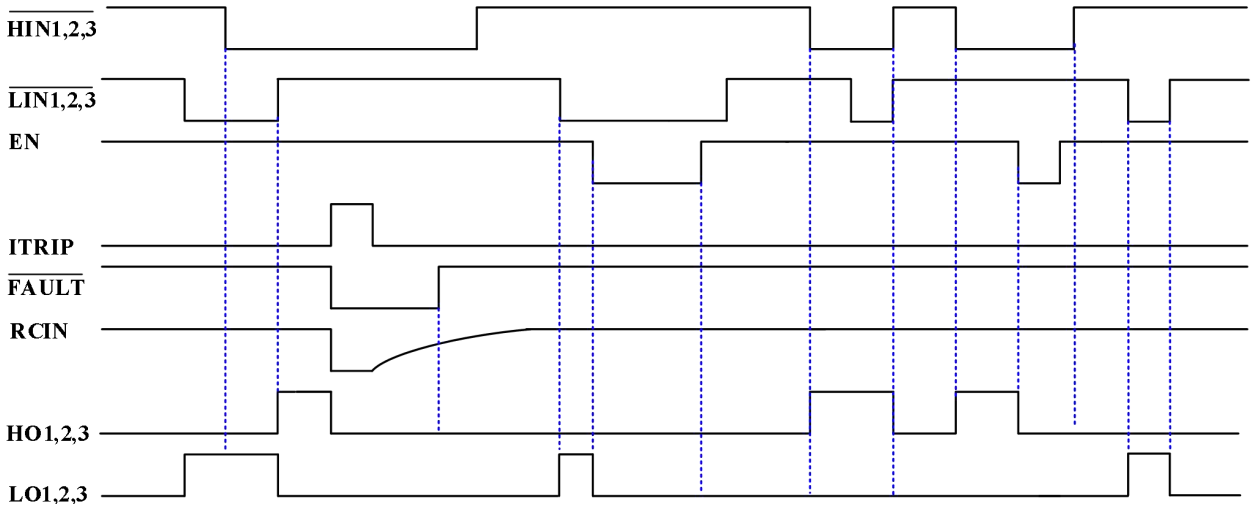


Figure 9-1. TPG2136 Input and output timing waveform

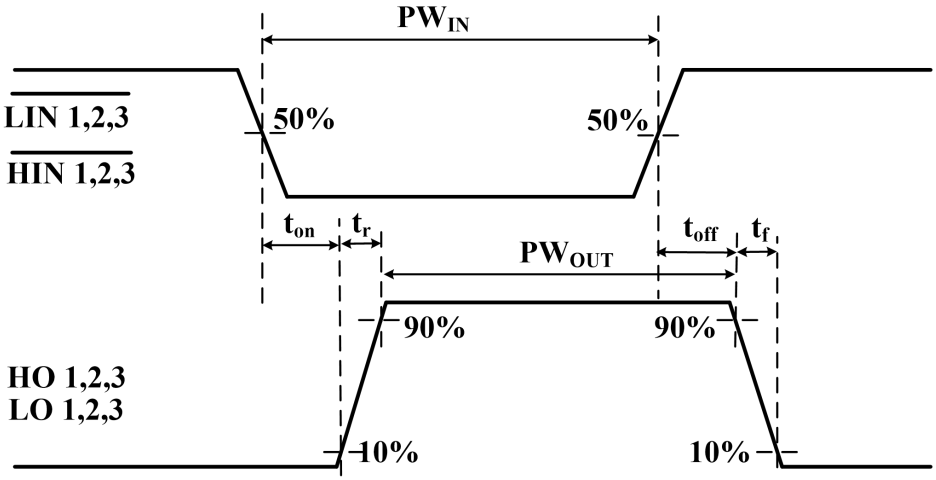


Figure 9-2. Propagation Time Waveform Definition

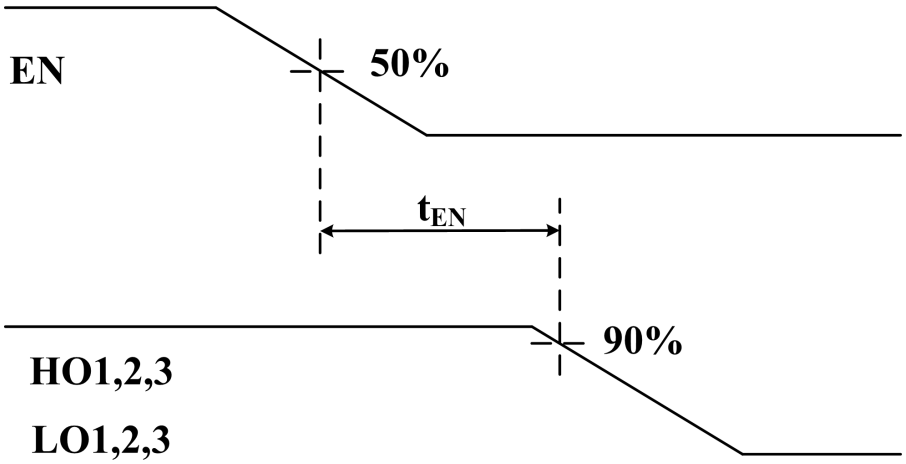


Figure 9-3. Output Enable Timing Waveform

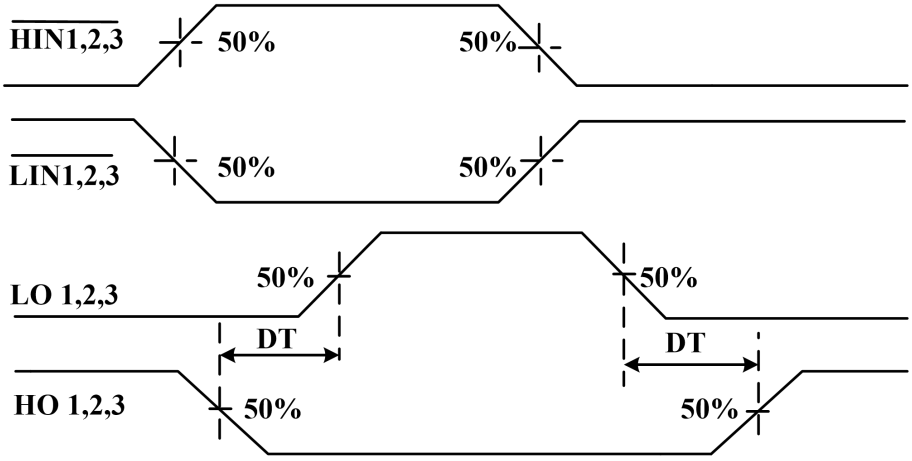


Figure 9-4. Cross Conduction Prevention Delay Time Waveform Definition

10 Description

10.1 Overview

TPG2136 is an N-type high-voltage, high-speed power MOSFET/IGBT high-low side three-phase gate driver chip, including three independent half-bridge driver circuits. The three-way high-side floating drive can operate in a system with a voltage above 700V through a bootstrap circuit, and can achieve 100% duty cycle under the condition that the VB-VS voltage is higher than the under voltage threshold.

The input end of TPG2136 is integrated with filtering function. When the input signal jitter occurs or the input pulse width is less than the filtering time, the output signal will remain unchanged. Both inputs are compatible with CMOS and TTL, making it easier to connect to the main control chip.

The TPG2136 includes a variety of protection features, including EN enable control, internal interlocking and over current detection. When the EN enable port is a low level signal, the driver chip does not trigger output under any conditions. The internal interlock function makes the driver chip not output high level signals in HO and LO at the same time, avoiding direct short circuit at the power output end of the bridge circuit. Over current detection can quickly detect the current change of the power device, so that the application works in a stable state.

At the same time, in order to meet various industrial design requirements, TPG2136 designed a programmable time restart port, through the parameter selection of the RC loop, you can freely choose the restart time within a certain width.

10.2 Function Block Diagram

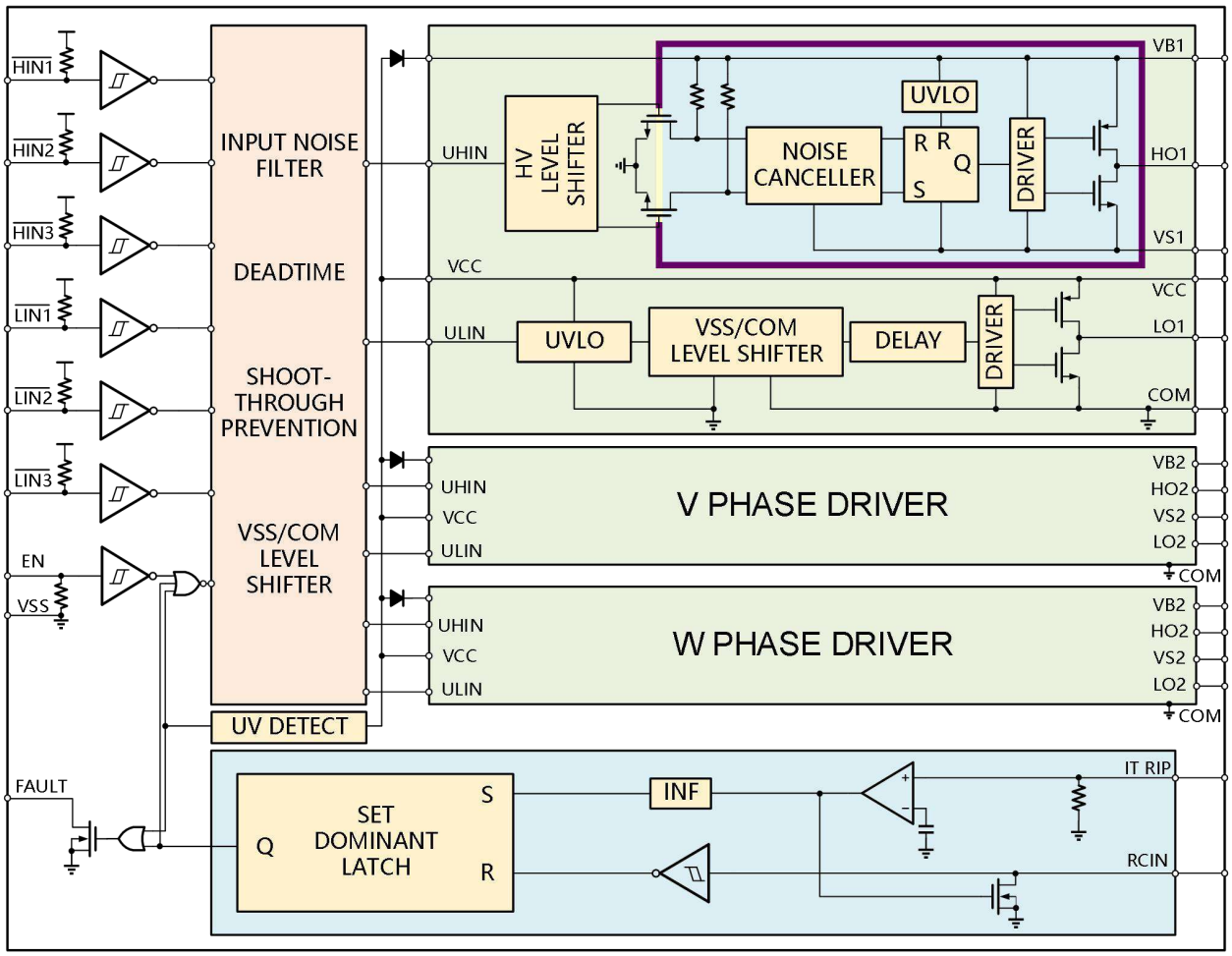


Figure10-1 Function Block Diagram of TPG2136

10.3 Chip static logic

The signal input ports (HIN and LIN) of TPG2136 adopt the edge trigger mode. When the chip is powered on and the status of each protection port is normal, the output will respond only when the signal of the input band edge is sent. The EN, ITRIP, and RCIN ports all use the level trigger mode, that is, the voltage meets the logical requirements, and the chip can work normally, as shown in Table 10-1.

Table 10-1 I/O logical table

INPUT					OUTPUT	
SIGNAL		SENSE				
HIN	LIN	EN	ITRIP	RCIN	HO	LO
X	X	L	X	X	L	L
P	P	H	L	H	L	L
P	N	H	L	H	L	H
N	P	H	L	H	H	L
N	N	H	L	H	L	L
X	X	H	H	L	L	L
X	X	H	L	L	L	L
Note: P stands for rising edge; N stands for falling edge; H stands for high level; L stands for low level						

10.4 Signal input port

The TPG2136 contains three independent half-bridge signal input ports for receiving control signals from the master without interfering with each other. There is an interlock function between the high side and the low side of each half bridge to ensure that the output of the high side and the low side of the same phase will not be high at the same time. And there is a built-in dead time between the high side and the low side signals, which effectively avoids serious faults caused by overlapping output signals. The signal input port adopts the mode of edge trigger, so after the trigger protection, the next trigger edge signal needs to be given before the output will change. Each signal input port is pulled down to the VSS through a 40KΩ resistor and is set to a low level input when floating. Each signal input port (including the EN enable port) contains a filtering function and will not be triggered by pulses lower than the filtering time. When the input signal of the port containing the filtering function changes, its duration is less than the input filtering time, and the output port is not affected. When the change duration of the input signal is longer than the input filtering time, the output port changes with the input signal and keeps the same time as the input signal, as shown in Figure 10-2:

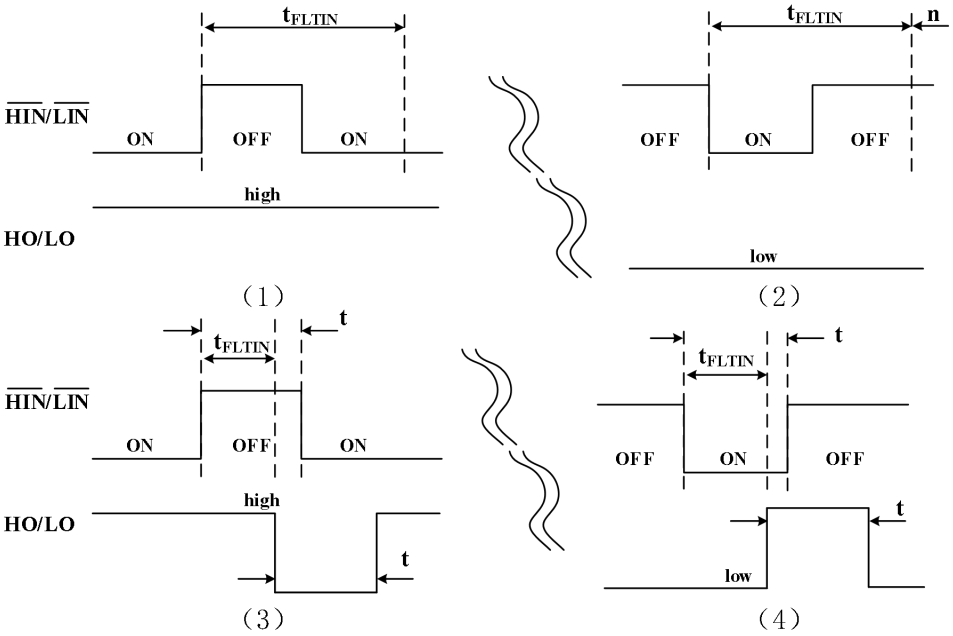


Figure 10-2 Input filter waveform definition

(1) When a positive pulse signal is input, and the pulse signal width is less than the filter width ($t < t_{FLTIN}$), as shown in Figure 10.2(1). The output signal does not change and continues to be high;
(2) When a positive pulse signal is input, and the pulse signal width is greater than the filter width ($t > t_{FLTIN}$), as shown in Figure 10.2(3). The output signal changes, triggering a low level with a duration of t (the same input pulse width time) and then resuming a high level;
(3) When a negative pulse signal is input, and the pulse signal width is less than the filter width ($t < t_{FLTIN}$), as shown in Figure 10.2(2). The output signal does not change and continues to be low;
(4) When a negative pulse signal is input, and the pulse signal width is greater than the filter width ($t > t_{FLTIN}$), as shown in Figure 10.2(4). The output signal changes, triggering a high level of duration t (the same input pulse width time) and then resuming the low level.

10. 5 Output port

The internal push-pull structure of the output port is used to directly drive the power device MOSFET/IGBT. The reference ground of the output port on the low side is COM, and the reference ground of the output port on the high side is VS. When VS is high voltage, the voltage domain between VB-VS needs to be powered by a bootstrap circuit to work normally. The VS pin has a certain negative pulse resistance, which can ensure that no damage occurs under the pulse condition of -9V, 50ns.

10. 6 Under voltage protection function

Both the high and low voltage drivers of the TPG2136 contain an under voltage protection circuit that monitors both the supply voltage (VCC) and the bootstrap capacitor voltage (VB-VS), and the UVLO circuit will suppress all outputs until the voltage is sufficient to drive the external MOSFETs (to the appropriate preset threshold). Therefore, when the voltage of the VCC pin rises above the UVLO threshold, all output ports remain low. When the bootstrap capacitor voltage (VB-VS) rises above the UVLO threshold, only the high-side output (HO) is disabled. When the under voltage protection function of VCC is triggered, the chip will return the $\overline{\text{FAULT}}$ pin to make its output low. When the high bootstrap capacitor voltage (VB-VS) is under voltage, it will not output the $\overline{\text{FAULT}}$ signal (low level) at the fault pin end.

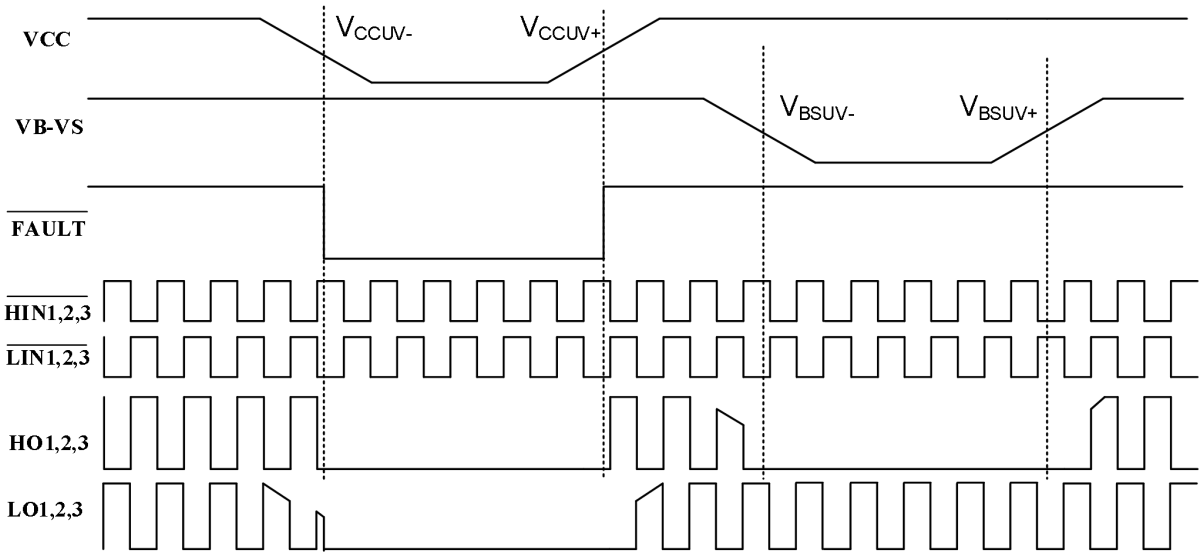


Figure10-3 Under voltage function waveform definition

As shown in Figure 10-3, when the VCC under voltage occurs, all output signals immediately become low. When the VCC voltage rises again to exceed the under voltage threshold, the output signal must be enabled only after the effective edge of the input signal. When the high-side bootstrap capacitor voltage (VB-VS) is reduced below the under voltage threshold, the high-side output immediately becomes low, and the LO output signal is not affected. When the high-side bootstrap capacitor voltage (VB-VS) rises above the under voltage threshold, the high-side signal also requires the effective edge of the input signal to enable the output. In addition, the threshold hysteresis of UVLO is built into the TPG2136. There is a certain hysteresis between the threshold of the power supply voltage drop to trigger the under voltage and the threshold of the voltage rebound chip to work normally, which can prevent abnormal output waveform when the power supply voltage fluctuates.

10.7 Enable

The TPG2136 has a built-in 1MΩ pull-down resistor between the EN pin and the VSS pin, so leaving the VSS pin afloat will cause the chip to fail to output properly. If you do not use the EN function, it is recommended to connect it to the VCC pin. If you need to use a pull-up resistor, you are advised to use a 10 Kω resistor to pull up the VCC pin, as shown in Figure 10-4. In environments with high electromagnetic noise, it is recommended to use a 1nf capacitor to connect the EN pin to the VSS pin and as close to the EN pin as possible. The EN pin has a built-in filtering function to protect it from pulse signals below the filtering enabled time.

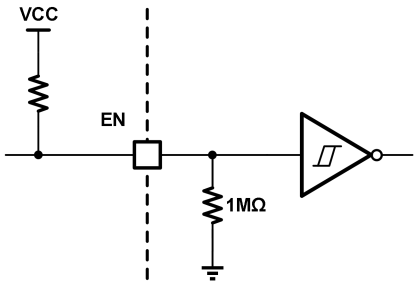


Figure 10-4 EN pin block diagram

10. 8 Over current protection function

The TPG2136 has a built-in 1MΩ pull-down resistance between the ITRIP pin and the VSS pin, so the ITRIP pin can be floated or connected to the VSS pin when over current protection is not in use. The ITRIP pin can be used to monitor the operating current of the MOSFET/IGBT by detecting the voltage across the sampling resistor.

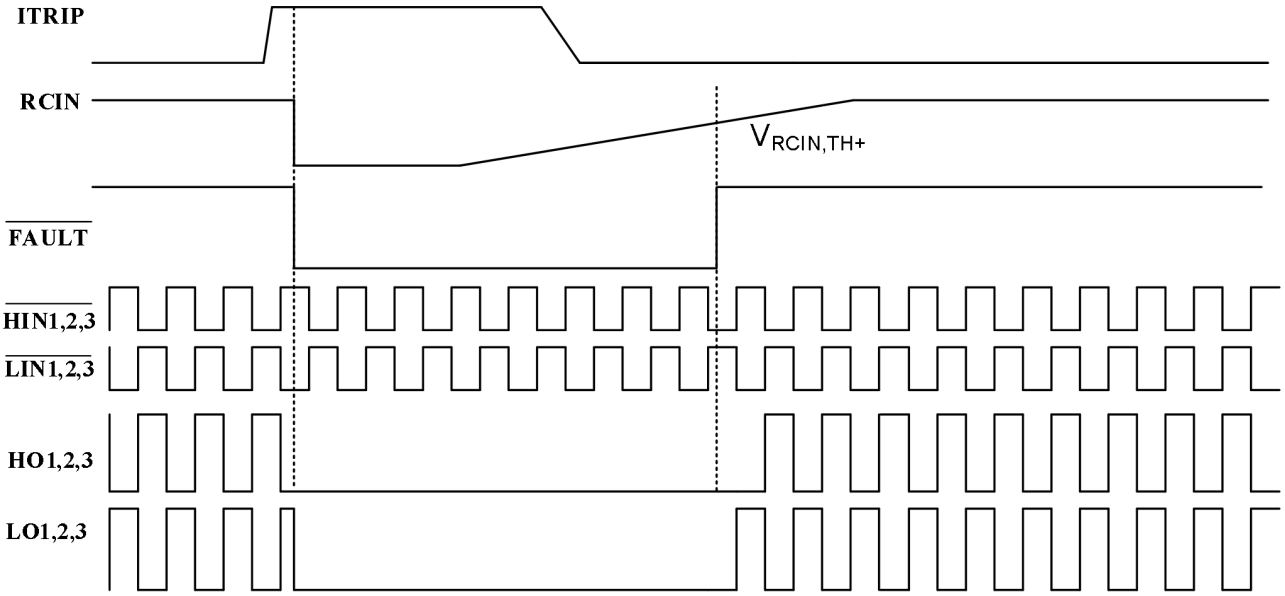


Figure 10-5 Waveform definition of over current protection

As shown in Figure 10-5, when a short circuit or over current occurs at the end of the power device, the ITRIP voltage rises to exceed the threshold voltage of over current protection, and after tbl for a period of time, the internal switch controls to lower the voltage of the RCIN pin, and returns an error signal to make the $\overline{\text{FAULT}}$ pin output low level and shut off all signal transmission channels. The output of all output ports is low, which effectively protects the application design. RCIN pin external RC timing circuit for programming $\overline{\text{FAULT}}$ recovery time, external resistance for external capacitor charge, RCIN pin voltage starts to rise, when RCIN reaches a certain threshold voltage, clear the fault pin signal, set to high level; At this time, the circuit is ready for normal work and waits for the arrival of the effective edge of the next input signal to enable the output signal. In addition, the built-in ITRIP hysteresis prevents abnormal output waveform when the current of the power device fluctuates.

RCIN fault delay function

When the ITRIP voltage rises to the trigger threshold, the MOS turns on to lower the RCIN pin voltage and the chip turns off the output function. When the ITRIP pin signal recovers below the threshold voltage, the VCC charges C1 through R2 (as shown in Figure 10-6) to gradually increase the RCIN pin voltage. When the RCIN pin voltage rises above the threshold voltage, the chip restores output function. Built-in RCIN hysteresis prevents abnormal fluctuations in the voltage waveform during charging.

It is recommended that the R2 resistance be set to 2MΩ, and the 1.6mS delay is used as an example.

$$C = \frac{t}{R * \ln\left(\frac{V_{CC}}{V_{CC} - V_{TH}}\right)}$$

$$C = \frac{1.6ms}{2M\Omega * \ln\left(\frac{15V}{15V - 8V}\right)} = 1.05nF$$

It is concluded that C1 value here is about 1nf, which can be appropriately reduced considering the possible leakage situation.

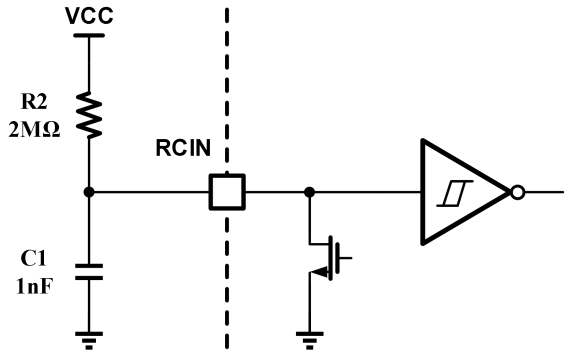


Figure 10-6 RCIN pin block diagram

10.9 Typical application circuit

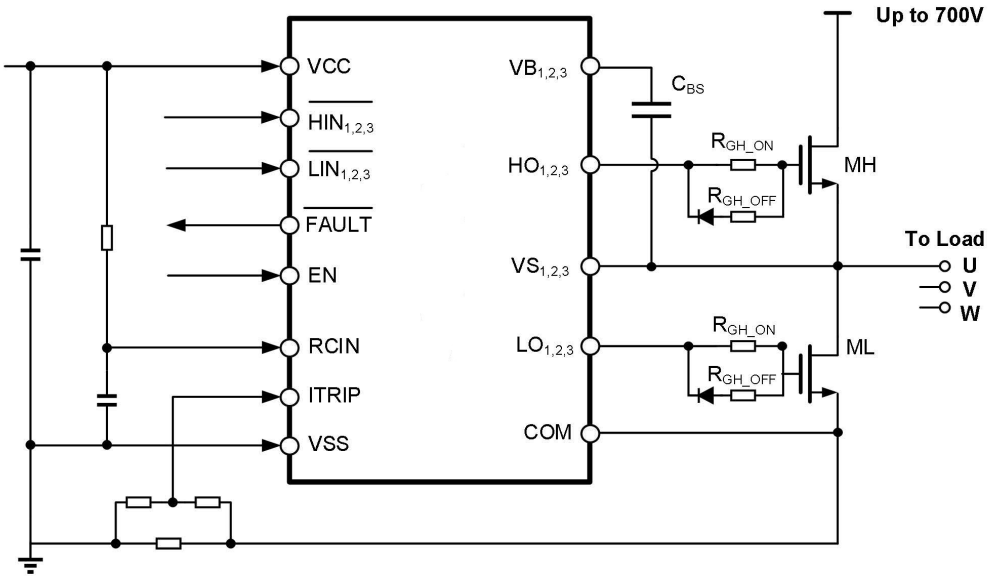


Figure10-7 Typical application circuit of TPG2136

10.9.1 Bootstrap Circuit Design Guide

Figure 10-8 shows the structure of a general half-bridge circuit, which consists of a bootstrap resistor, bootstrap diode, and bootstrap capacitor. This scheme is the most commonly used and cost-effective scheme in the current motor drive.

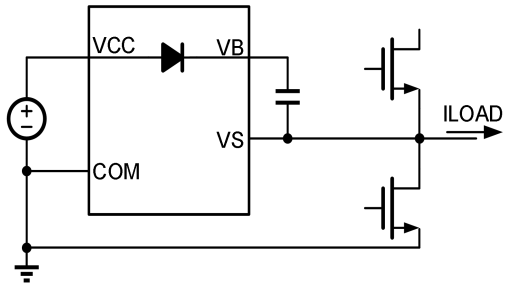


Figure 10-8 Basic structure of the bootstrap circuit

Bootstrap circuit capacitance selection

In order to determine the size of the bootstrap capacitance, we first need to evaluate the following points：

-The gate charge required for MOS to turn on: Q_g;

-GS leakage of MOS: I_{LK_GS};

-Static operating current of the drive: I_{QBS};

-Leakage of bootstrap diode: I_{LK_DIODE};

-Bootstrap capacitor leakage: I_{LK_CAP};

-Upper bridge height time: T_{HON}.

I_{LK_CAP} is included in the calculation only when the bootstrap capacitor uses an electrolytic capacitor. Other types of capacitors do not need to be considered. It is recommended to use at least one low ESR ceramic capacitor. Parallel electrolytic capacitor and low ESR ceramic capacitor can achieve better circuit performance.

By calculation, we can find the loss of capacitance for a single turn on：

$$Q_{TOT} = Q_G + (I_{LK\_GS} + I_{QBS} + I_{LK\_DIODE} + I_{LK\_CAP}) \times T_{HON}$$

Specifies the range that VBS can drop during bootstrapping: $\triangle V_{BS}$

$$\Delta V_{BS} \leq V_{CC} - V_F - V_{GSmin} - V_{DSon}$$

In the process, you need assurance：

$$V_{GSmin} > V_{BSUV-}$$

V_F MOS reverse diode voltage drop

V_{GEmin} Maintain the minimum gate voltage for MOS tube conduction

V_{DSon} On-off pressure drop of the lower bridge MOS

And with that, you can calculate it：

$$C_{BOOTmin} = \frac{Q_{TOT}}{\triangle V_{BS}}$$

Note: In the process of calculating bootstrap capacitance here, only the charge required for a pulse process is calculated, without considering the duty ratio and frequency of PWM. If the signal is controlled by PWM wave, please get the actual required bootstrap capacitance size based on the above calculation method through a certain equivalent conversion.

Note on bootstrap circuit

A. Bootstrap resistance

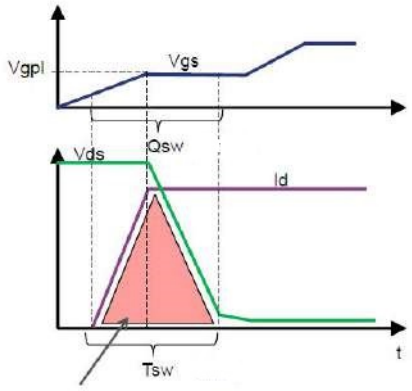
Bootstrap resistors are used in some bootstrap circuits and are not required. HO and LO may have abnormal jump during startup. At this time, the increase of bootstrap resistance will limit the current passing through the bootstrap diode when the bootstrap circuit is started, which can effectively suppress some bad signals and protect the circuit.

10.9.2 Bootstrap circuit capacitance selection

Gate resistance is used to control the switching speed of the driven MOS and the slope of the rising and falling edge, which will affect a number of application performance, such as loss, reliability and so on. This section describes how to select the driving resistance and discusses the impact of the driving resistance. The selection of grid resistance is closely related to the driver chip, MOSFET and even circuit design, and it needs to be re-selected according to the actual situation in different environments.

Common industrial brushless motors operate at a frequency of about 2kHz-10kHz. Based on this, grid resistors of 20-120 Ω are usually selected. This is determined by the following two factors：

（1） **Switching loss of MOS.** Part of the MOS loss is switching loss, and the other part is on-off loss, while the grid resistance mainly affects the loss of the switching process. The larger the resistance value, the slower the switching process, and the larger the overlap area of voltage and current, the greater the loss. The most direct impact of excessive loss is that the chip temperature will rise rapidly, and the device will face the risk of failure under the condition of higher than 150℃.



$$Psw(on) = \frac{1}{2} \times Id \times Vds \times Tsw(on)$$

Figure 10-9 MOS switch loss under resistive load

（2） **Reliability.** As opposed to loss, the smaller the resistance value of the gate resistance, the faster the MOSFET will switch. In practical applications, the power end current is larger, more sensitive to parasitic parameters, too high switching speed will increase the signal instability, light will make the motor EMI is too large, heavy will make the circuit damage. Some of the most common are:

1) Grid signal rings, causing MOS damage (as shown in Figure 10-10);

2) The dv/dt is too fast, and the VS port will bear too high or too low voltage signal, resulting in drive damage.

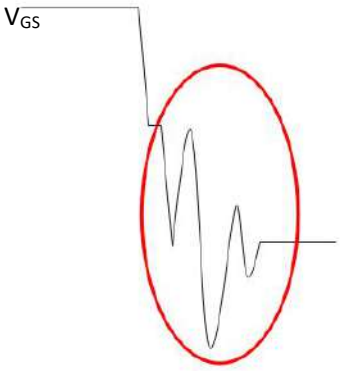


Figure 10-10 Grid ringing

10-10 PCB layout guide

To achieve the outstanding performance of half bridge grid driver chips, the following printed circuit board (PCB) layout routing guidelines should be followed.

• Low ESR/ESL capacitors should be placed near the driver chip between the VCC and COM pins, and between the VB and VS pins to provide peak current for the VCC and VB pins.

• To prevent large voltage transients from high-side MOSFET drains, a low ESR electrolytic capacitor and a ceramic capacitor must be connected between the high-side MOSFET drain and the ground (COM).

• To avoid excessive negative voltage transients on switch node (VS) pins, the parasitic inductance between the high-side MOSFET source and the low-side MOSFET (synchronous rectifier) source must be minimized.

• Overlap of the VS layer with the ground (COM) layer should be avoided as much as possible to minimize the coupling of switching noise from the VS layer to the ground layer.

• The heat dissipation pad of the driver chip should be connected to a large area of thick copper layer to improve the heat dissipation performance of the driver chip. The heat dissipation pad is usually connected to the ground that is equal to the COM of the chip. It is recommended to connect the heat dissipation pad to the COM pin only.

• Grounding precautions:

The primary goal of designing a ground connection is to limit the MOSFET gate charge and discharge loop to the smallest possible loop area. This method reduces the loop inductance and can effectively avoid the noise problem on the MOSFET gate. At the same time, the gate driver chip should be as close to the MOSFET as possible.

The second consideration is to ensure reasonable charging paths for bootstrap capacitors, including VCC bypass capacitors based on ground (COM), bootstrap diodes, bootstrap capacitors, and low-side MosFETs. Since the VCC bypass capacitor charges the bootstrap capacitor by cycle through the bootstrap diode, and each charge occurs in a very short period of time, this charge path passes through the peak current. Minimizing the loop length and area of the bootstrap circuit on PCB can make the bootstrap circuit work in a stable state, which is very important to ensure the reliable operation of the driver chip.

11 Package Information

SOP28 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	2.65	D	17.89	18.09	18.29
A1	0.10	-	0.30	E	10.10	10.30	10.50
A2	2.25	2.30	2.35	E1	7.30	7.50	7.70
A3	0.97	1.02	1.07	e		1.27BSC	
b	0.39	-	0.48	L	0.70	-	1.00
b1	0.38	0.41	0.43	L1		1.40BSC	
c	0.25	-	0.31	θ	0	-	8°
c1	0.24	0.25	0.26				

SOP28 Package Outlines