TPG2186 700V Half Bridge MOSFET/IGBT Gate Driver

1 Features and Benefits

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Undervoltage lockout for both channels
  --UVLO forward 8.9V
  --UVLO reverse 8.2V
- Turn-on/Turn-off propagation delay
  -- Ton/Toff =130ns/130ns
- Matched propagation delay for both channels
- Typically output Source/Sink current capability: 4A/4A
- RoHS compatible

2 Application

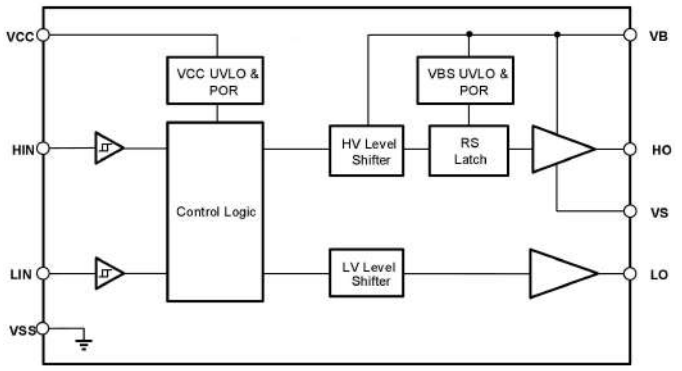
- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

3 Description

The TPG2186 is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700 V.

Part Number	Package	Body size
TPG2186	SOIC8	4.9mm x 3.9mm

Functional Block Diagram



4 Selection Guide

Part No.	High-side input	Low-side input	Anti-cross	Dead-time	VBS UVLO	Ton/Toff (ns)	IO+/IO- (A)
TPG2186	HIN	LIN	NO	--	YES	130/130	4.0/4.0

5 Ordering Guide

Part Number	Input logic	Package	Package	SPQ
TPG2186	G2186 XXXXXX	SOIC8	Tape & Reel	4000

6 Revision history

Version	Content	Time
V1.0	Create	2021.11.29
V2.0	Product features and application information	2022.03.17
V2.1	Update maximum working voltage	2022.9.29
V2.2	Update turn-on rise time and tun-off fall time	2023.05.09

7 Function Pin Description

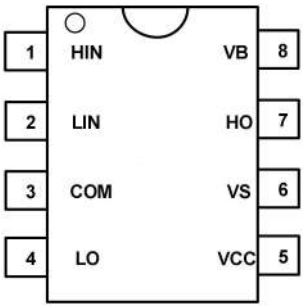


Figure7-1 8-Pin SOIC8 Top view

Table7-1 Lead Definitions

Number	Symbol	Description
1	HIN	Logic input for high side gate driver output (HO), in phase
2	LIN	Logic input for low side gate driver output (LO), in phase
3	COM	Low side return
4	LO	Low side gate drive output
5	VCC	Low side and logic fixed supply
6	VS	High side floating supply return
7	HO	High side gate drive output
8	VB	High side floating supply

8 Product specifications

8.1 Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to COM and an ambient temperature of 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	-0.3	725	V
V_S	High side floating supply return	V_B - 25	V_B + 0.3	
V_{HO}	High side gate drive output	V_S -0.3	V_B + 0.3	
V_{CC}	Low side and main power supply	-0.3	25	
V_{LO}	Low side gate drive output	-0.3	V_{CC} + 0.3	
V_{IN}	Logic input（HIN, LIN）	-0.3	V_{CC} + 0.3	

8.2 ESD rating

Symbol	Definition	MIN.	MAX.	Units
ESD	HBM Model	1.5	—	kV
	Machine Model	500	—	V

8.3 Rated power

Symbol	Definition	MIN.	MAX.	Units
P_D	Package Power Dissipation @ TA ≤25°C	—	0.625	W

8.4 Thermal information

Symbol	Definition	MIN.	MAX.	Units
Rth_{JA}	Thermal Resistance, Junction to Ambient	—	200	°C /W
T_J	Junction Temperature	—	150	°C
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (Soldering, 10 seconds)	—	300	

8.5 Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and COM are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to COM and the ambient temperature is 25°C.

Symbol	Definition	MIN.	MAX.	Units
V_B	High side floating supply	VS + 10	VS + 20	V
V_S	High side floating supply return	-9	700	
V_{HO}	High side gate drive output	V_S	V_B	
V_{CC}	Low side and main power supply	10	20	
V_{LO}	Low side gate drive output	0	VCC	
V_{IN}	Logic input of HIN & LIN	0	VCC	
T_A	Ambient temperature	-40	125	°C

8. 6 Electrical Characteristics

Valid for temperature range at T_A= 25ºC, V_{CC}=V_B= 15V, C_L=1nF, unless otherwise specified

8.6.1 Dynamical electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
t_{ON}	Turn-on propagation delay	—	130	250	ns	VS=0
t_{OFF}	Turn-off propagation delay	—	130	250		VS=0V or 700V
t_R	Turn-on rise time	—	15	20		VS=0V
t_F	Turn-off fall time	—	10	15		
MT	Matched propagation time delay	—	—	50		

8.6.2 Static electrical characteristics

Symbol	Definition	MIN.	TYP.	MAX.	Units	Test Condition
V_{CCUV+}	VCC supply UVLO threshold	8	8.9	9.8	V	
V_{CCUV-}		7.4	8.2	9.0		
$V_{CCUVHYS}$	hysteresis of V_{CC} UVLO	—	0.7	—		
V_{BSUV+}	VBS supply UVLO threshold	8	8.9	9.8		
V_{BSUV-}		7.4	8.2	9.0		
$V_{BSUVHYS}$	hysteresis of V_{BS} UVLO	—	0.7	—		
I_{LK}	High-side floating supply leakage current	—	—	50	μA	VB=VS=700V
I_{QBS}	Quiescent VB supply current	—	50	100		VIN=0V or 5V
I_{QCC}	Quiescent VCC supply current	—	150	240		
V_{IH}	Quiescent VDD supply current	2.5	—	—	V	VCC=10~20V
V_{IL}	Logic “1” input voltage	—	—	0.8		
V_{OH}	Logic “0” input voltage	—	—	1.4		IO=0A
V_{OL}	High level output voltage, VBIAS - VO	—	—	0.1		IO=20mA
I_{IN+}	Low level output voltage, VO	—	25	60	μA	LIN=5V,
I_{IN-}	Logic “1” Input bias current	—	—	2		LIN=0V,
I_{O+}	Logic “0” Input bias current	3.0	4.0	—	A	Vo=0V PW≤10μs
I_{O-}	Output high short circuit pulsed current	3.0	4.0	—		Vo=15V PW≤10μs

9 Function Description

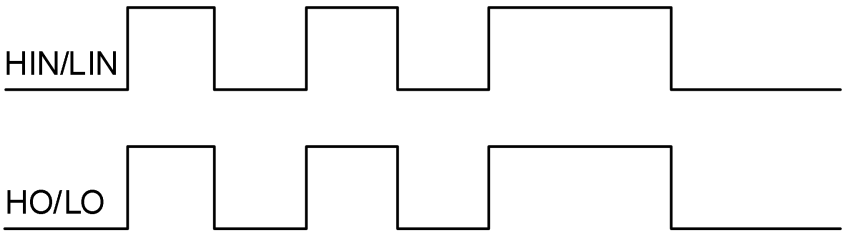


Figure 9-1 TPG2186 Input and output timing waveform

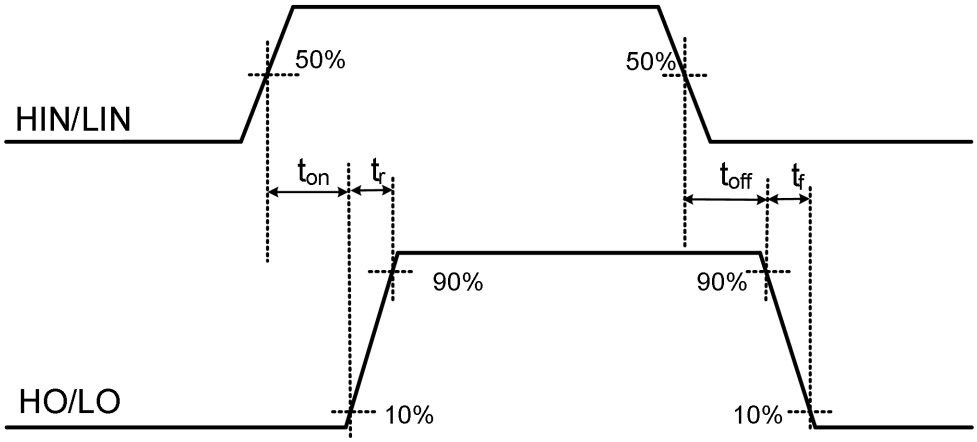


Figure 9-2 Propagation Time Waveform Definition

10 Description

10.1 Function Block Diagram

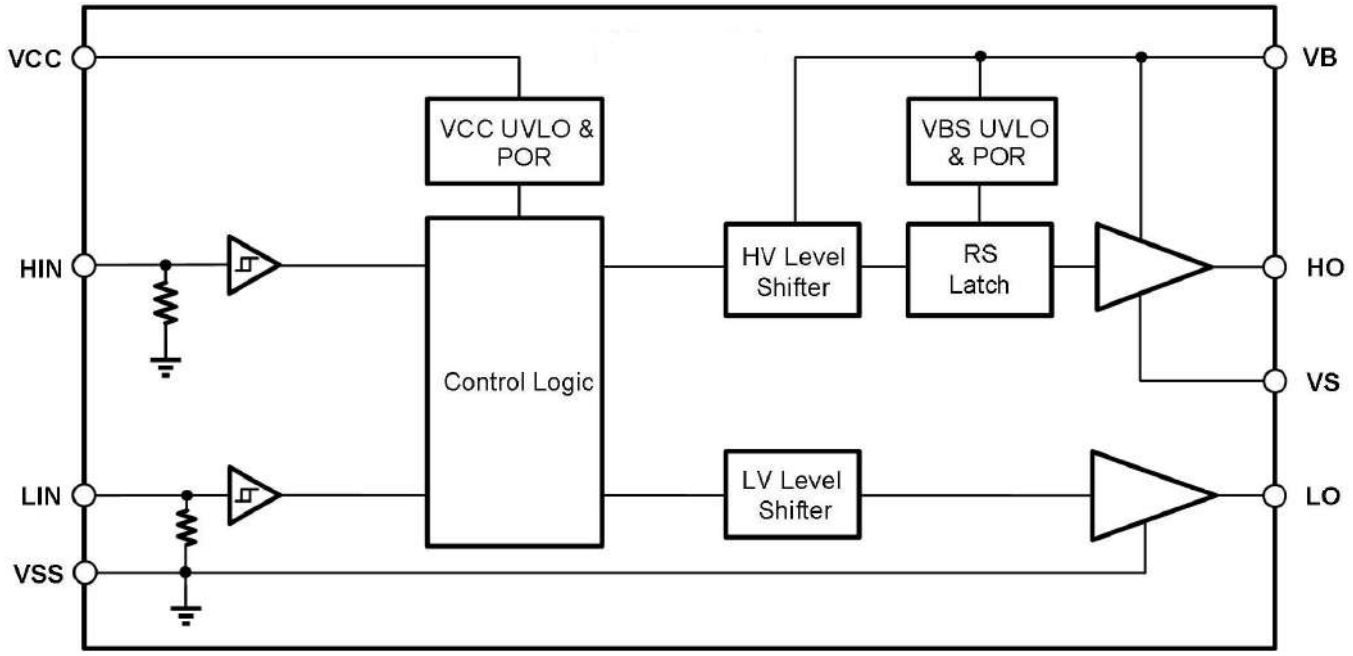


Figure 10-1 Function Block Diagram of TPG2186

10. 2 Application message

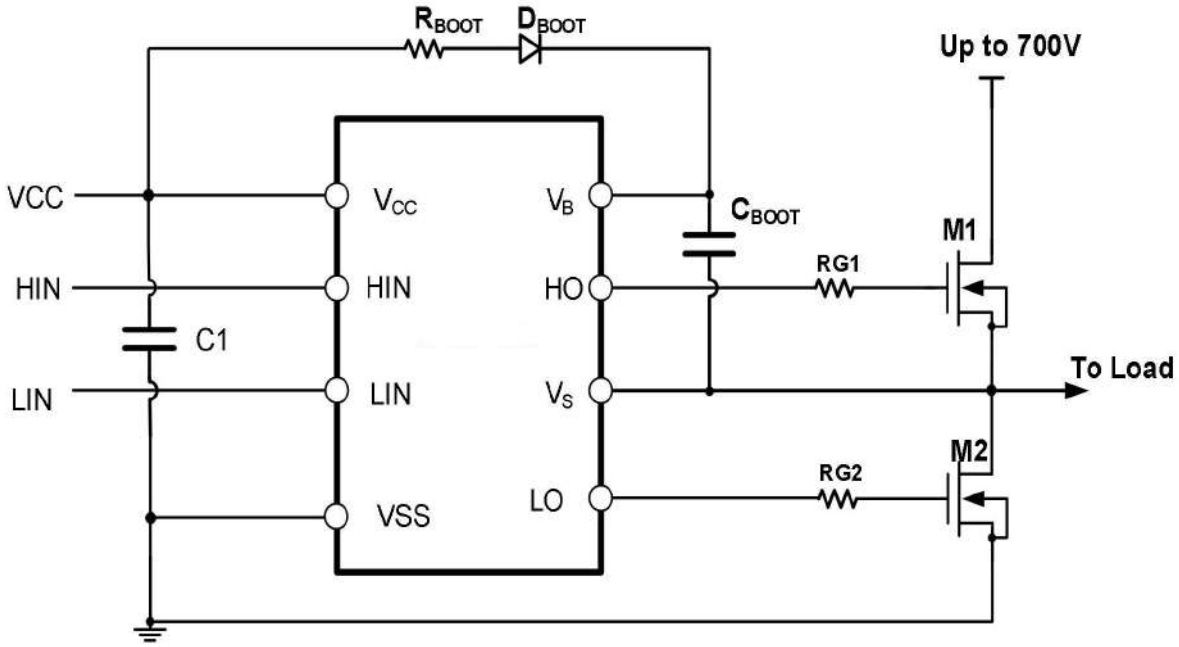


Figure10-2 Typical application circuit of TPG2186

11. Package Information

SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

SOIC-8 Package Outlines