TPG27524 Dual 4A High-Speed Power Switching Driver

1 Features

- Latch Protection: withstand 0.5 A reverse current
- Ability to Handle Negative Voltages (-10 V) at Inputs
- Low Output Impedance
- Two Independent Gate-Drive Channel
- Independent-Enable Function for Each Output
- 4-A Peak Source and Sink-Drive Current
- 4.5 to 20-V Single-Supply Range
- High Ability of driving capacitive load:
  -- Switch time at 1nF load < 25ns
- Rise/Fall time matching
- Fast Propagation Delays (40-ns Typical)
- Operating Temperature Range of -40 to 125°C
- Turn on/Turn off Delays:
  -- Ton/Toff =70ns/70ns
- The RoSH Standard
  SOIC8/DFN8

2 Applications

- line drivers
- Pulse transformer driver
- Driving MOSFETs and IGBTs
- Motor drives
- pulse generator
- Switch-Mode Power Supplies
- DC-to-DC Converters
- class D switching amplifier

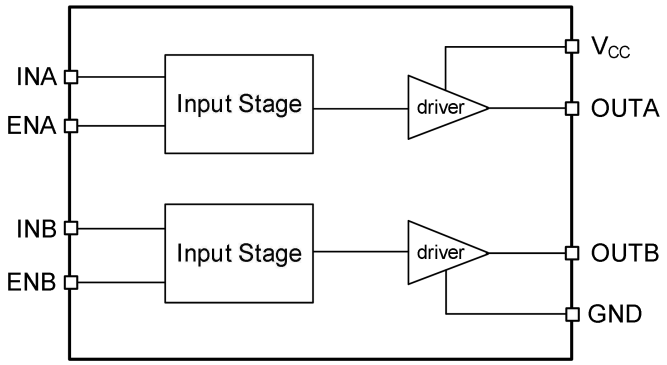
3 Description

The TPG27524 device is a dual-channel, high-speed, low-side, gate-driver device capable of effectively driving MOSFET and IGBT power switches. It has a matching rise and fall time when charging and discharging the gate of the power switch. In addition, TPG27524 has a high degree of latch resistance under all conditions in its rated power and voltage range. TPG27524 is not damaged when noise spikes (any polarity) of up to 5V appear on the ground pin. TPG27524 can accept up to 500mA of reverse current without causing damage or logic confusion. All terminals are fully protected by ESD up to 2.0 kV.

Device Information

PART NUMBER	PACKAGE	BODY SIZE(NOM)
TPG27524	SOIC8	4.9mm x 3.9mm

Pin Configuration



4 Product Selection

Product Type	Input-Output Phase	Package	Ton/Toff (ns)
TPG27524	In-phase	8-PIN SOIC	40/40

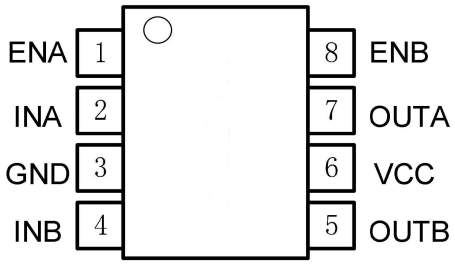
5 Ordering Information

Product Type	Mark	Package	Form	Min Quantity
TPG27524	G27524 XXXXXX	SOIC8	Reel	4 K/R

6 Revision History

Version	History	Date
V1.0	create	2021.11.29
V2.0	Product features and application information	2022.04.01
V2.1	Update the maximum operating voltage	2022.09.29

7 Pin Configuration and Functions



8-Pin SOIC8 Package Top View

Pin Functions

PIN	NAME	DESCRIPTION
1	ENA	Enable input for Channel A: ENA is biased LOW to disable the Channel A output regardless of the INA state. ENA is biased HIGH or left floating to enable the Channel A output. ENA is allowed to float; hence the pin-to-pin compatibility with the TPG27524 N/C pin.
2	INA	Input to Channel A: INA is the non-inverting input in the TPG27524 device. OUTA is held LOW if INA is unbiased or floating.
3	GND	Ground: All signals are referenced to this pin.
4	INB	Input to Channel B: INA is the non-inverting input in the TPG27524 device. OUTB is held LOW if INB is unbiased or floating.
5	OUTB	Output of Channel B
6	VCC	Bias supply input
7	OUTA	Output of Channel A
8	ENB	Enable input for Channel B: ENB is biased LOW to disable the Channel B output regardless of the INB state. ENB is biased HIGH or left floating to enable the Channel B output. ENB is allowed to float; hence the pin-to-pin compatibility with the TPG27524 N/C pin.

8 Specifications

8.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

Symbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	—	25	V
V_{IN}	INA, INB voltage	GND-10	V_{CC}+0.3	

8.2 ESD Ratings

Symbol	Definition	MIN	MAX	UNIT
ESD	Human body model (HBM)	—	2000	V
	Charged device model (CDM)	—	500	V

8.3 Power Ratings

Symbol	Definition	MIN	MAX	UNIT
PD	SOIC package power(TA ≤70°C)	—	470	mW

8.4 Thermal Information

S mbol	Definition	MIN	MAX	UNIT
T_J	Operating junction temperature	—	+150	°C
T_S	Storage temperature	-45	+150	

8.5 Recommended Operating Conditions

To properly operate, device should be used in the following recommended conditions. All voltages are with respect to GND unless otherwise noted, Currents are positive into, negative out of the specified terminal, environment temperature is 25 ℃.

S mbol	Definition	MIN	MAX	UNIT
V_{CC}	Supply voltage range	4.5	20	V
T_C	ambient temperature	-40	125	°C

8.6 Electrical Characteristics

TA= 25℃, 4.5V ≤VCC≤18V (unless otherwise noted)

Symbol	Definition	MIN	TYP	MAX	UNIT
V_{IH}	Input signal high threshold	2.4	—	—	V
V_{IL}	Input signal low threshold	—	—	0.8	V
I_{IN}	Input current(0V≤V_{IN}≤V_{CC})	—	—	300	μA
V_{OH}	High output voltage	V_{CC}–0.025	—	—	V
V_{OL}	Low output voltage	—	—	0.025	V
R_{OH}	Output pullup resistance(V_{CC}=18V,I_O=100mA)	—	0.7	—	Ω
R_{OL}	Output pulldown resistance(V_{CC}=18V,I_O=100mA)	—	04	—	Ω
I_{PK}	Peak output source current	—	4	—	A
I_{REV}	Reverse current that latch protection can withstand (Working cycle≤2%,t≤300us,V_{CC}=18V)	—	>0.5	—	A
t_R	Rise time(V_{CC}=18V,C_{LOAD}=100pF)	—	—	15	ns
t_F	Fall time(V_{CC}=18V,C_{LOAD}=100pF)	—	—	15	ns
t_{ON}	Turn-on propagation delay(V_{CC}=18V,C_{LOAD}=100pF)	—	25	40	ns
t_{OFF}	Turn-off propagation delay(V_{CC}=18V,C_{LOAD}=100pF)	—	25	40	ns
t_{EN}	Enable propagation delay(V_{CC}=18V,C_{LOAD}=100pF)	—	25	40	ns
I_{Q1}	VCC quiescent supply current(V_{INA}=V_{INB}=HIGH)	—	—	1.5	mA
I_{Q0}	VCC quiescent supply current(V_{INA}=V_{INB}=LOW)	—	—	1.5	mA

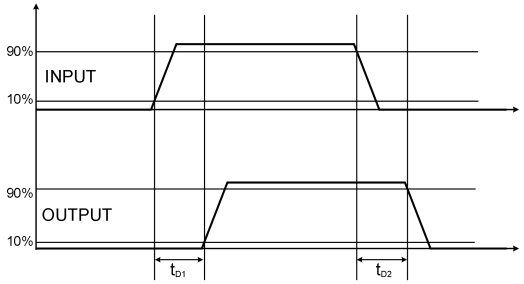


Figure 1 Input-Output waveform(non-inverting)

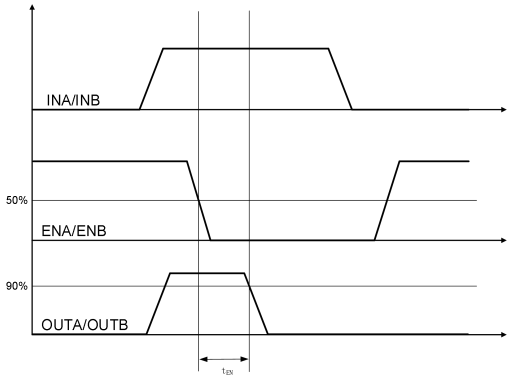


Figure 2 Enable Function waveform

8.7 Typical Characteristics

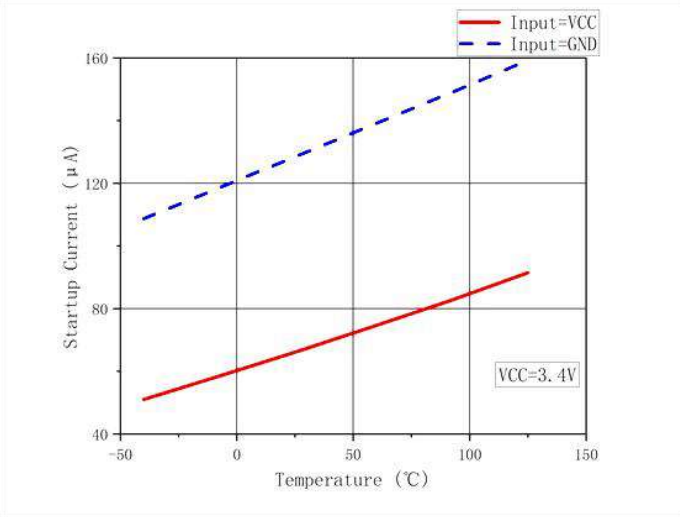


Figure 3. Start-Up Current vs Temperature

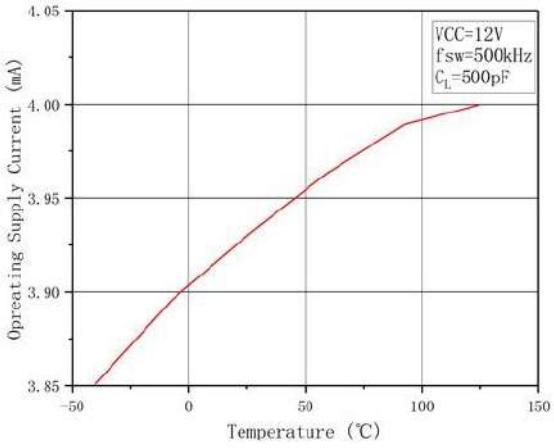


Figure 4. Operating Supply Current vs Temperature (Outputs Switching)

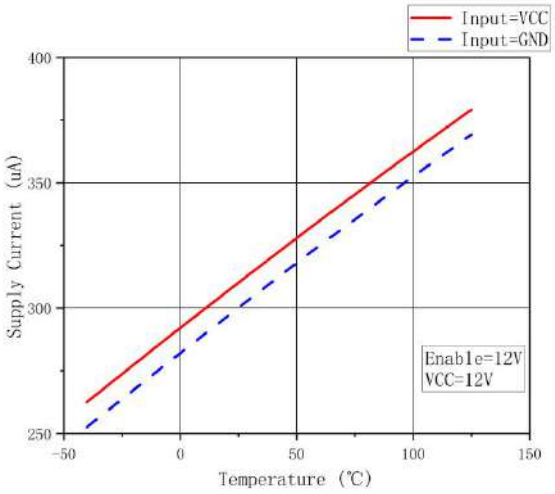


Figure 5. Supply Current vs Temperature (Outputs In DC On/Off Condition)

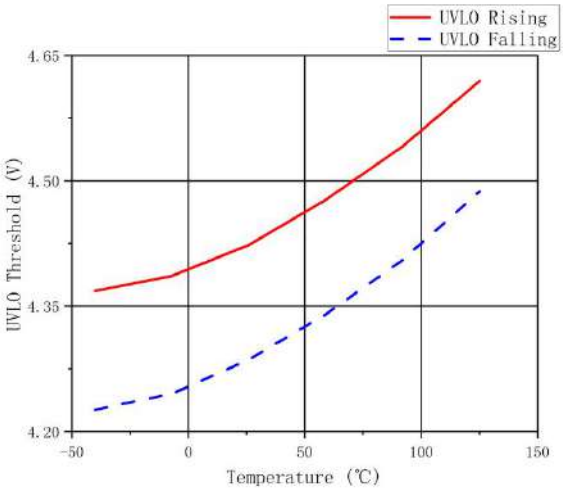


Figure 6. UVLO Threshold vs Temperature

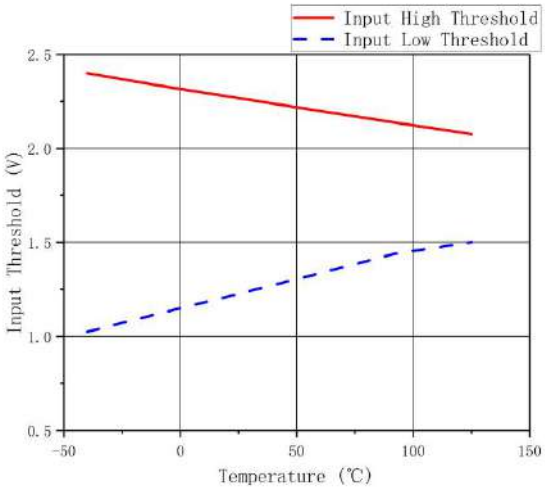


Figure 7. Input Threshold vs Temperature

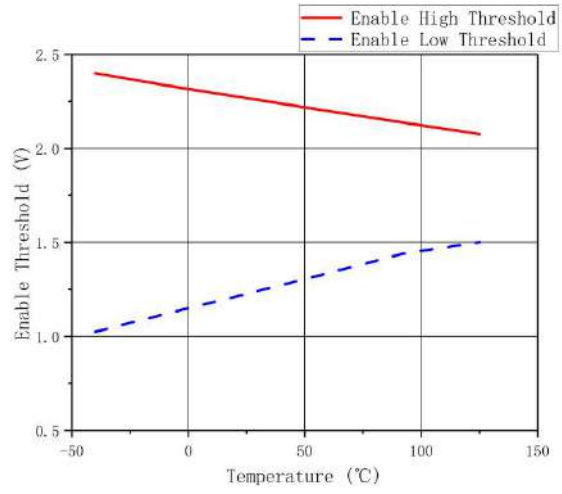


Figure 8. Enable Threshold vs Temperature

Typical Characteristics(continued)

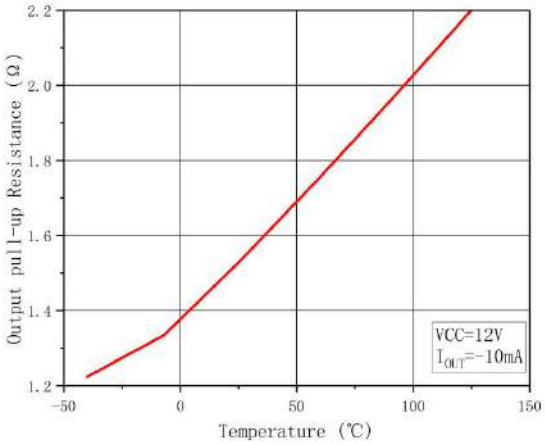


Figure 9. Output Pull-up Resistance vs Temperature

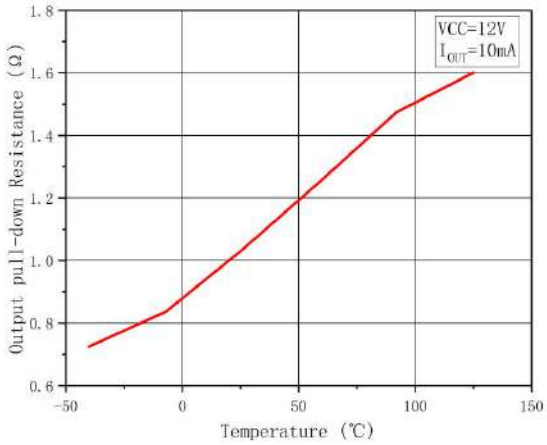


Figure 10. Output Pull-down Resistance vs Temperature

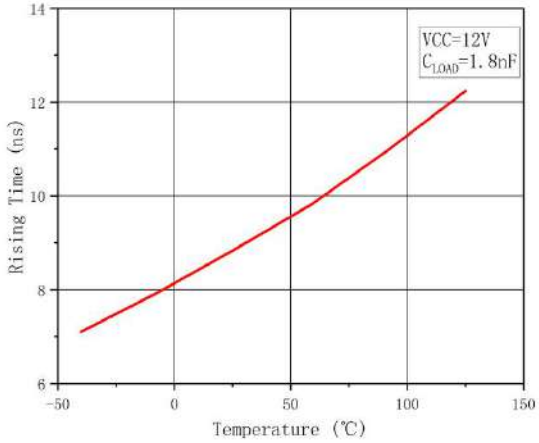


Figure 11. Rise Time vs Temperature

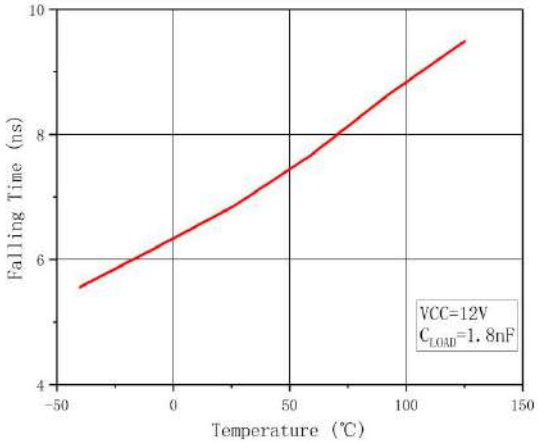


Figure 12. Fall Time vs Temperature

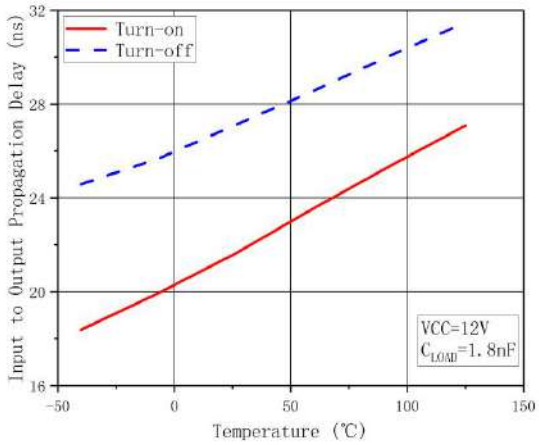


Figure 13. Input to Output Propagation Delay vs Temperature

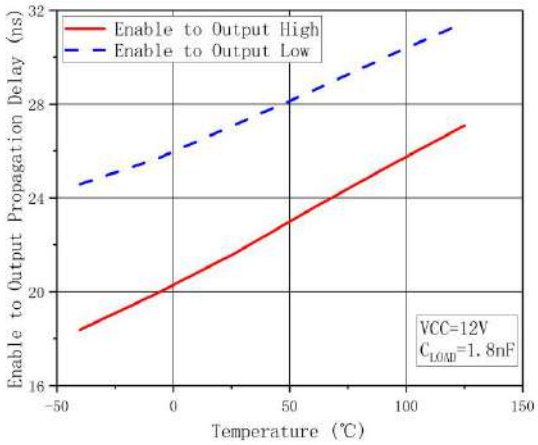


Figure 14. En to Output Propagation Delay vs Temperature

Typical Characteristics(continued)

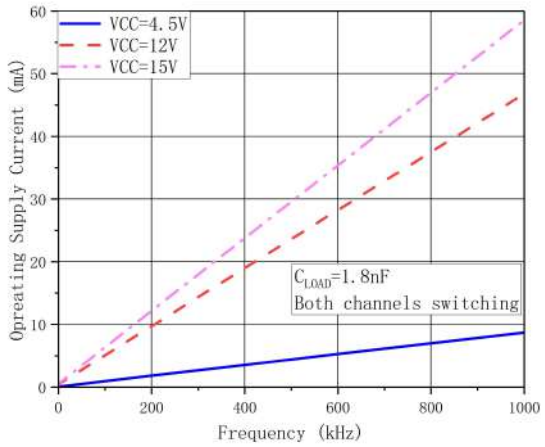


Figure 15. Operating Supply Current vs Frequency

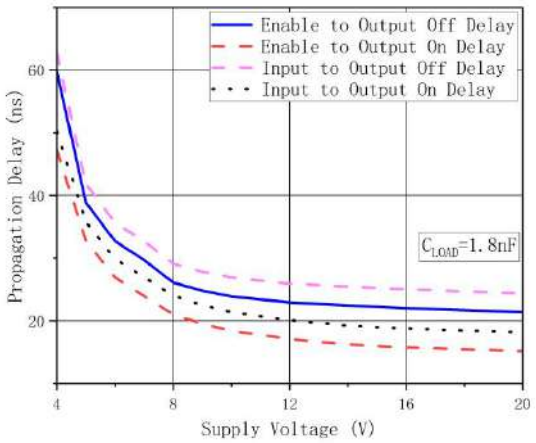


Figure 16. Propagation Delays vs Supply Voltage

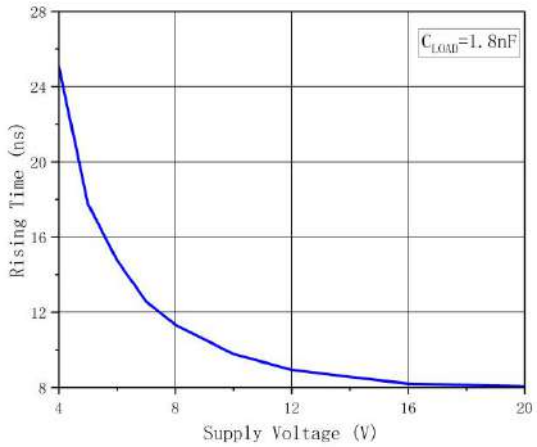


Figure 17. Rise Time vs Supply Voltage

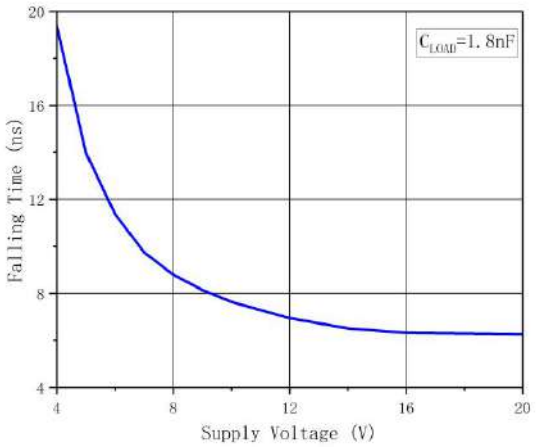


Figure 18. Fall Time vs Supply Voltage

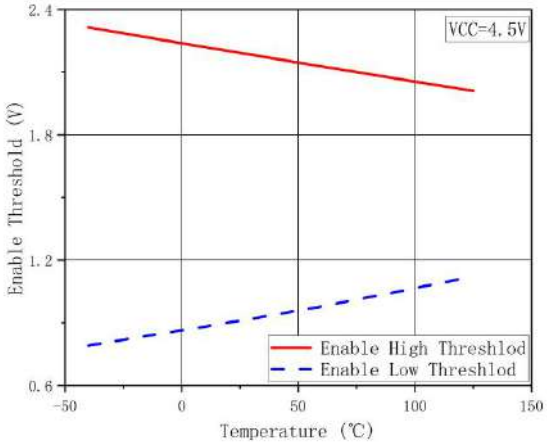
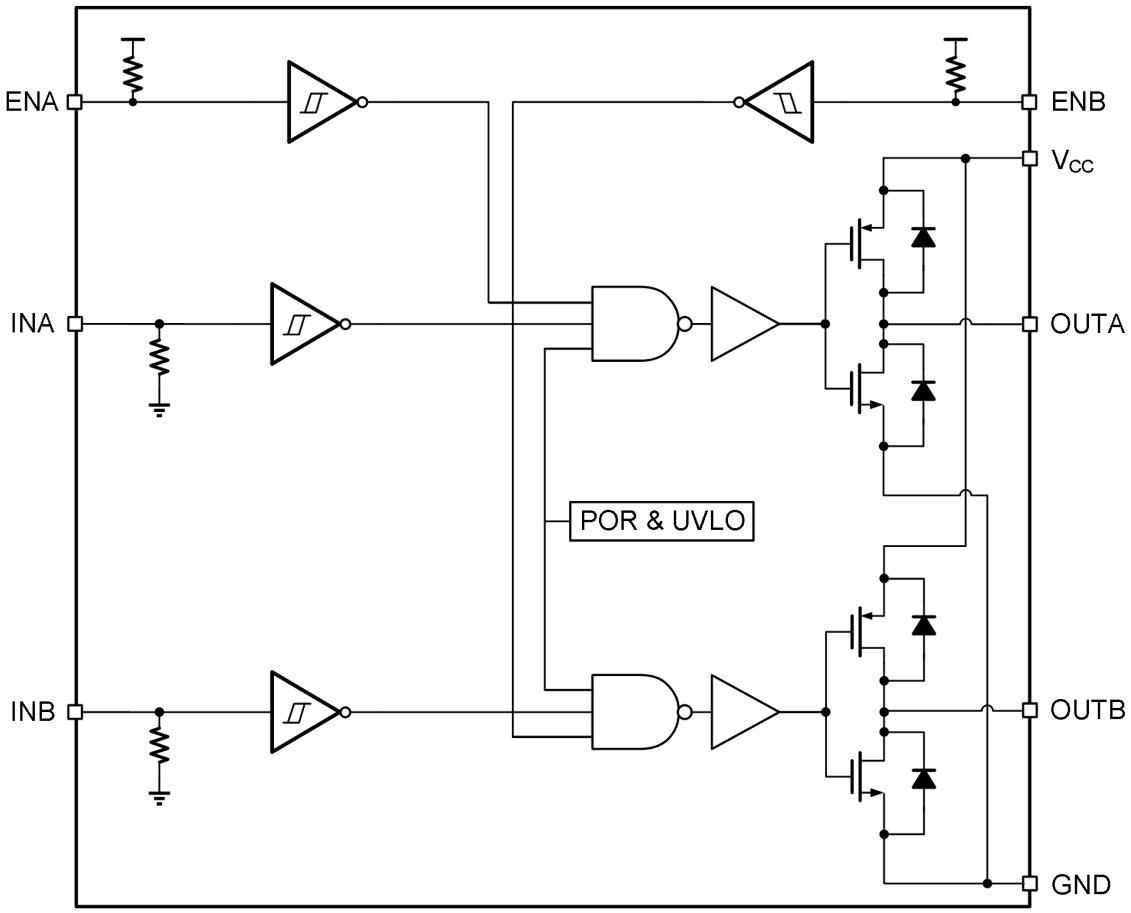


Figure 19. Enable Threshold vs Temperature

9 Detailed description

9.1 Functional Block Diagram



9.2 Feature description

9.2.1 Input Stage

The input pins of TPG27524 gate-driver devices are based on a TTL and CMOS compatible input-threshold logic that is independent of the VCC supply voltage. With typically high threshold = 2.4 V and typically low threshold = 0.8 V, the logic level thresholds are conveniently driven with PWM control signals derived from 3.3-V and 5-V digital power-controller devices. TPG27524 devices also feature tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 9). The very low input capacitance on these pins reduces loading and increases switching speed.

The input stage of each driver is driven by a signal with a short rise or fall time. This condition is satisfied in typical power supply applications, where the input signals are provided by a PWM controller or logic gates with fast transition times (<200 ns) with a slow changing input voltage, the output of the driver may switch repeatedly at a high frequency. While the wide hysteresis offered in TPG27524 definitely alleviates this concern over most other TTL input threshold devices, extra care is necessary in these implementations. If limiting the rise or fall times to the power device is the primary goal, then an external resistance is highly recommended between the output of the driver and the power device. This external resistor has the additional benefit of reducing part of the gate-charge related power dissipation in the gate driver device package and transferring it into the external resistor itself.

9.2.2 Enable Function

The enable function is an extremely beneficial feature in gate-driver devices especially for certain applications such as synchronous rectification where the driver outputs disable in light-load conditions to prevent negative current circulation and to improve light-load efficiency.

TPG27524 device is provided with independent enable pins ENx for exclusive control of each driver-channel operation. The enable pins are based on a non-inverting configuration (active-high operation). Thus when ENx pins are driven high the drivers are enabled and when ENx pins are driven low the drivers are disabled. Like the input pins, the enable pins are also based on a TTL and CMOS compatible input-threshold logic that is independent of the supply voltage and are effectively controlled using logic signals from 3.3-V and 5-V microcontrollers. The TPG27524 devices also feature tight control of the Enable-function threshold-voltage levels which eases system design considerations and ensures stable operation across temperature (refer to Figure 8). The ENx pins are internally pulled up to VCC using pullup resistors as a result of which the outputs of the device are enabled in the default state.

9.2.3 Output Stage

The TPG27524 device output stage features a unique architecture on the pullup structure which delivers the highest peak-source current when it is most needed during the Miller plateau region of the power-switch turn-on transition (when the power switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-Channel MOSFET and an additional N-Channel MOSFET in parallel. The function of the N-Channel MOSFET is to provide a brief boost in the peak sourcing current enabling fast turn-on. This is accomplished by briefly turning-on the N-Channel MOSFET during a narrow instant when the output is changing state from Low to High.

The ROH parameter (see Electrical Characteristics) is a DC measurement and it is representative of the onresistance of the P-Channel device only. This is because the N-Channel device is held in the off state in DC condition and is turned-on only for a narrow instant when output changes state from low to high. Note that effective resistance of the TPG27524 pullup stage during the turnon instant is much lower than what is represented by ROH parameter.

The pulldown structure in the TPG27524 device is simply composed of a N-Channel MOSFET. The ROL parameter (see Electrical Characteristics), which is also a DC measurement, is representative of the impedance of the pulldown stage in the device. In the TPG27524 device, the effective resistance of the hybrid pullup structure during turnon is estimated to be approximately 1.5 × ROL, estimated based on design considerations.

Each output stage in the TPG27524 device is capable of supplying 4-A peak source and 4-A peak sink current pulses. The output voltage swings between VCC and GND providing rail-to-rail operation, thanks to the MOSoutput stage which delivers very low drop-out. The presence of the MOSFET-body diodes also offers low impedance to switching overshoots and undershoots which means that in many cases, external Schottky-diode clamps may be eliminated. The outputs of these drivers are designed to withstand 500-mA reverse current without either damage to the device or logic malfunction.

The TPG27524 device is particularly suited for dual-polarity, symmetrical drive-gate transformer applications where the primary winding of transformer driven by OUTA and OUTB, with inputs INA and INB being driven complementary to each other. This situation is because of the extremely low drop-out offered by the MOS output stage of these devices, both during high (VOH) and low (VOL) states along with the low impedance of the driver output stage, all of which allow alleviate concerns regarding transformer demagnetization and flux imbalance. The low propagation delays also ensure accurate reset for high-frequency applications.

For applications that have zero voltage switching during power MOSFET turnon or turnoff interval, the driver supplies high-peak current for fast switching even though the miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before power MOSFET is switched on.

9.2.4 Low Propagation Delays And Tightly Matched Outputs

The TPG27524 driver device features a best in class, 40-ns (typical) propagation delay between input and output which goes to offer the lowest level of pulse-transmission distortion available in the industry for high frequency switching applications. For example in synchronous rectifier applications, the SR MOSFETs are driven with very low distortion when a single driver device is used to drive both the SR MOSFETs.

Caution must be exercised when directly connecting OUTA and OUTB pins together because there is the possibility that any delay between the two channels during turnon or turnoff may result in shoot-through current conduction. While the two channels are inherently very well matched, note that there may be differences in the input threshold voltage level between the two channels which causes the delay between the two outputs especially when slow dV/dt input signals are employed. The following guidelines are recommended whenever the two driver channels are paralleled using direct connections between OUTA and OUTB along with INA and INB:

• Use very fast dV/dt input signals (20 V/μs or greater) on INA and INB pins to minimize impact of differences in input thresholds causing delays between the channels.

• INA and INB connections must be made as close to the device pins as possible.

Wherever possible, a safe practice would be to add an option in the design to have gate resistors in series with OUTA and OUTB. This allows the option to use 0-Ω resistors for paralleling outputs directly or to add appropriate series resistances to limit shoot-through current, should it become necessary.

9.3 Device Functional Modes

Table 1 Device Logic Table

ENA	ENB	INA	INB	OUTA	OUTB
H	H	L	L	L	L
H	H	L	H	L	H
H	H	H	L	H	L
H	H	H	H	H	H
L	L	Any	Any	L	L
Any	Any	x(1)	x(1)	L	L
x(1)	x(1)	L	L	L	L
x(1)	x(1)	L	H	L	H
x(1)	x(1)	H	L	H	L
x(1)	x(1)	H	H	H	H

(1) Floating condition.

10 Applications and Implementation

10.1 Application Information

High-current gate-driver devices are required in switching power applications for a variety of reasons. In order to effect the fast switching of power devices and reduce associated switching-power losses, a powerful gate-driver device employs between the PWM output of control devices and the gates of the power semiconductor devices. Further, gate -driver devices are indispensable when it is not feasible for the PWM controller device to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which is not capable of effectively turning on a power switch. A level-shifting circuitry is required to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer-drive circuits based on NPN/PNP bipolar transistors in a totem-pole arrangement, as emitter-follower configurations, prove inadequate with digital power because the traditional buffer-drive circuits lack level-shifting capability. Gate-driver devices effectively combine both the level-shifting and buffer-drive functions. Gate-driver devices also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controller devices by moving gate-charge power losses into the controller. Finally, emerging wide band-gap power-device technologies such as GaN based switches, which are capable of supporting very high switching frequency operation, are driving special requirements in terms of gate-drive capability. These requirements include operation at low VCC voltages (5 V or lower), low propagation delays, tight delay matching and availability in compact, low-inductance packages with good thermal capability. In summary, gate-driver devices are an extremely important component in switching power combining benefits of high-performance, low-cost, component-count, board-space reduction, and simplified system design.

10.2 Typical Application

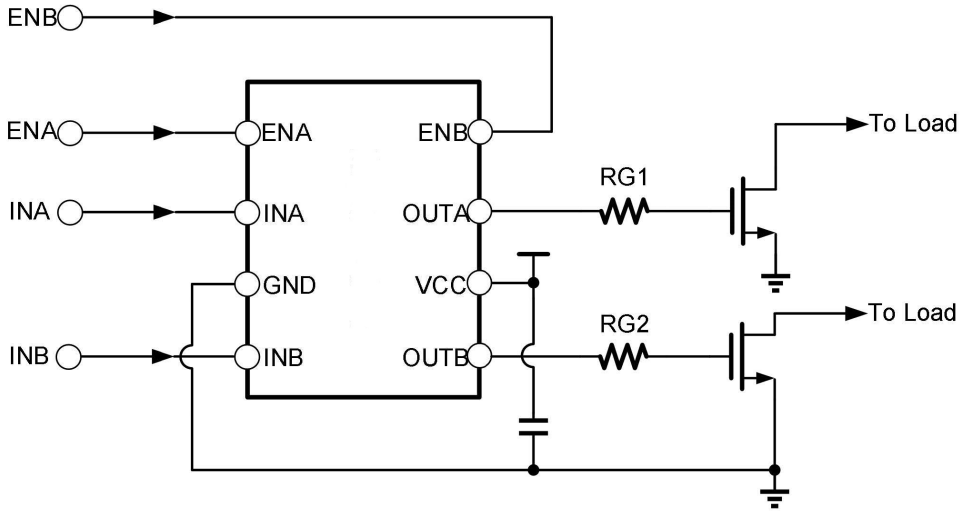


Figure 20 Inverting Typical Application Diagram of TPG27524

10.2.1 Design Requirements

When selecting the proper gate driver device for an end application, some desiring considerations must be evaluated first in order to make the most appropriate selection. Among these considerations are VCC, UVLO, Drive current and power dissipation.

10.2.2 Detailed Design Procedure

10.2.2.1 VCC and Undervoltage Lockout

The TPG27524 device has an internal undervoltage-lockout (UVLO) protection feature on the VCC pin supply circuit blocks. When VCC is rising and the level is still below UVLO threshold, this circuit holds the output low, regardless of the status of the inputs. The UVLO is typically 4.5 V with 100-mV typical hysteresis. This hysteresis prevents chatter when low VCC supply voltages have noise from the power supply and also when there are droops in the VCC bias voltage when the system commences switching and there is a sudden increase in IDD. The capability to operate at low voltage levels such as below 5 V, along with best in class switching characteristics, is especially suited for driving emerging GaN power semiconductor devices.

Because the device draws current from the VCC pin to bias all internal circuits, for the best high-speed circuit performance, two VCC bypass capacitors are recommended to prevent noise problems. The use of surface mount components is highly recommended. A 0.1-µF ceramic capacitor must be located as close as possible to the VCC to GND pins of the gate-driver device. In addition, a larger capacitor (such as 1-µF) with relatively low ESR must be connected in parallel and close proximity, in order to help deliver the high-current peaks required by the load. The parallel combination of capacitors presents a low impedance characteristic for the expected current levels and switching frequencies in the application.

10.2.2.2 Drive Current and Power Dissipation

The TPG27524 driver is capable of delivering 4-A of current to a MOSFET gate for a period of several-hundred nanoseconds at VCC = 12 V. High peak current is required to turn the device ON quickly. Then, to turn the device OFF, the driver is required to sink a similar amount of current to ground which repeats at the operating frequency of the power device. The power dissipated in the gate driver device package depends on the following factors:

• Gate charge required of the power MOSFET (usually a function of the drive voltage VGS, which is very close to input bias supply voltage VCC due to low VOH drop-out)

• Switching frequency

• Use of external gate resistors

Because TPG27524 features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver can be safely assumed to be negligible.

When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 1.

$$E_G=\frac{1}{2}C_{LOAD}V_{CC}^2$$

where

• C_{LOAD} is the load capacitor

• VCC is the bias voltage feeding the driver (1)

There is an equal amount of energy dissipated when the capacitor is charged. This leads to a total power loss given by equation 2.

$$P_G=C_{LOAD}V_{CC}^2f_{SW}$$

where

• f_{SW} is the switching frequency (2)

With VCC = 12 V, C_{LOAD} = 10 nF and f_{SW} = 300 kHz the power loss is calculated with equation 3

$$P_G=10nF\times12V^2\times300kHz=0.432W \quad (3)$$

The switching load presented by a power MOSFET is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications that provide the typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Q_g, the power that must be dissipated when charging a capacitor is determined which by using the equivalence $Q_g = C_{LOAD}$VCC to provide Equation 4 for power:

$$P_G=C_{LOAD}V_{CC}^2f_{SW}=Q_gV_{CC}f_{SW} \quad (4)$$

Assuming that the TPG27524 device is driving power MOSFET with 60 nC of gate charge (Q_g = 60 nC at VCC = 12 V) on each output, the gate charge related power loss is calculated with equation 5.

$$P_G=2\times60nC\times12V\times300kHz=0.432W \quad (5)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET turns on or turns off. Half of the total power is dissipated when the load capacitor is charged during turn-on, and the other half is dissipated when the load capacitor is discharged during turnoff. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor in accordance to the ratio of the resistances (more power dissipated in the higher resistance component). Based on this simplified analysis, the driver power dissipation during switching is calculated as follows (see equation 6):

$$P_G=0.5\times Q_GV_{CC}f_{SW}\times\left(\frac{R_{OFF}}{R_{OFF}+R_{GATE}}+\frac{R_{ON}}{R_{ON}+R_{GATE}}\right)$$

where

• R_{OFF} = R_{OL}

• R_{ON} (effective resistance of pullup structure) = 1.5×R_{OL} (6)

In addition to the above gate-charge related power dissipation, additional dissipation in the driver is related to the power associated with the quiescent bias current consumed by the device to bias all internal circuits such as input stage (with pullup and pulldown resistors), enable, and UVLO sections. As shown in Figure 4, the quiescent current is less than 0.6 mA even in the highest case. The quiescent power dissipation is calculated easily with equation 7.

$$P_Q=I_{DD}V_{DD} \quad (7)$$

Assuming , I_{CC} = 6 mA, the power loss is:

$$P_Q=0.6mA\times12V=7.2mW \quad (8)$$

Clearly, this power loss is insignificant compared to gate charge related power dissipation calculated earlier. With a 12 -V supply, the bias current is estimated as follows, with an additional 0.6-mA overhead for the quiescent consumption:

$$I_{CC}\sim\frac{P_G}{V_{CC}}=\frac{0.432W}{12V}=0.036A \quad (9)$$

11. PACKAGING INFORMATION

SOIC-8 Package Dimensions

Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)	Size / Symbol	MIN(mm)	TYP(mm)	MAX(mm)
A	-	-	1.75	D	4.70	4.90	5.10
A1	0.10	-	0.225	E	5.80	6.00	6.20
A2	1.30	1.40	1.50	E1	3.70	3.90	4.10
A3	0.60	0.65	0.70	e		1.27BSC	
b	0.39	-	0.48	h	0.25	-	0.50
b1	0.38	0.41	0.43	L		0.50	
c	0.21	-	0.26	L1	1.05BSC		
c1	0.19	0.20	0.21	θ	0	-	8°

SOIC-8 Package Outlines